

Gold Coast- MT / DT

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CK505 CLOCK Gen

VRD12 / VRM / Linear

XDP

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PCIe 16x slot X1

PCIe Gen2 16x

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Intel PROCESSOR
SANDY BRIDGE
LGA1155

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CHANNEL A DDR3 SDRAM (1066/1333)

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DDR3 DIMM 1
DDR3 DIMM 3

CHANNEL B DDR3 SDRAM (1066/1333)

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DDR3 DIMM 2
DDR3 DIMM 4

DISPLAY PORT

DP Link

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VGA CONN

VGA

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PCI Slot X1

PCI

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PCIe 16x Slot X1
(wired as 4x signal)

PCIe Gen2 4x

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PCIe 1x Slot X1

PCIe Gen2 1x

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XDP

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SATA 3.0 CONN X1

SATA Port 0

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SATA 2.0 CONN X2

SATA Port 1/ 2

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SATA 2.0 CONN X1 (MT)

SATA Port 3

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SPI ROM
2M+8M

SPI

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FDI

DMI

Intel
Cougar Point

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PCIe 1x

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Intel
Lewisville

NIC + USB
Ports X 2

Port 0/1

Port 2 ~ 5

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Port 6/7/10/11

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Port 8/9

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Rear USB Ports X4

Front USB Ports X4

Internal USB
Header X1

HDA

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ALC269Q

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Rear Audio CONN
Line In (MIC In)/Line Out

Front Audio CONN
HP Out/ MIC In

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LPC

SMSC5544

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TPM/TCM

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(TCM is just reserved because
MRD has removed TCM requirement)

SERIAL
Ports X2

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PS2
KB/MS

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Printer
Port

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DELL INC.

Title
Index / Block diagram

DWG NO

Gold Coast_MT/DT

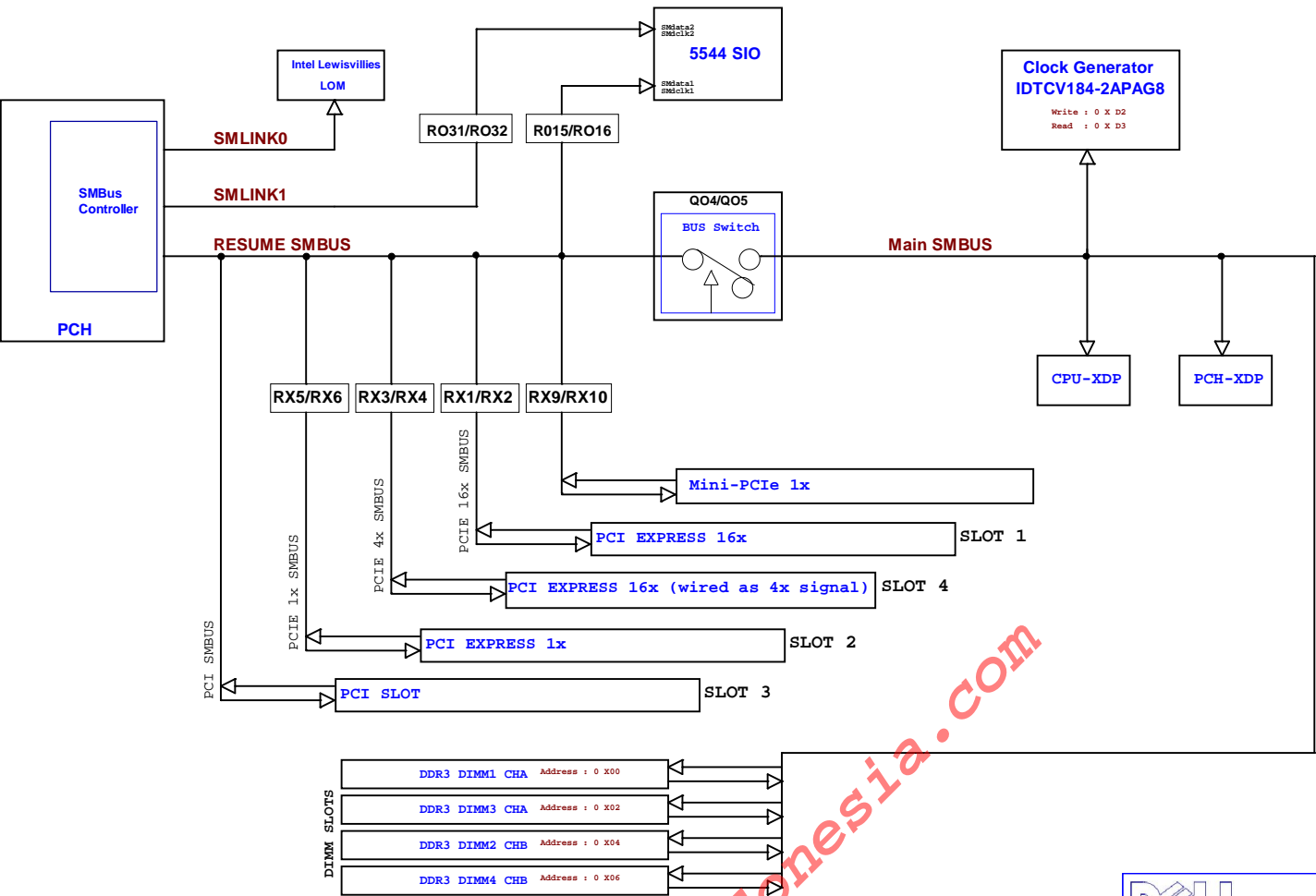
Rev
A00

Date: Friday, December 24, 2010

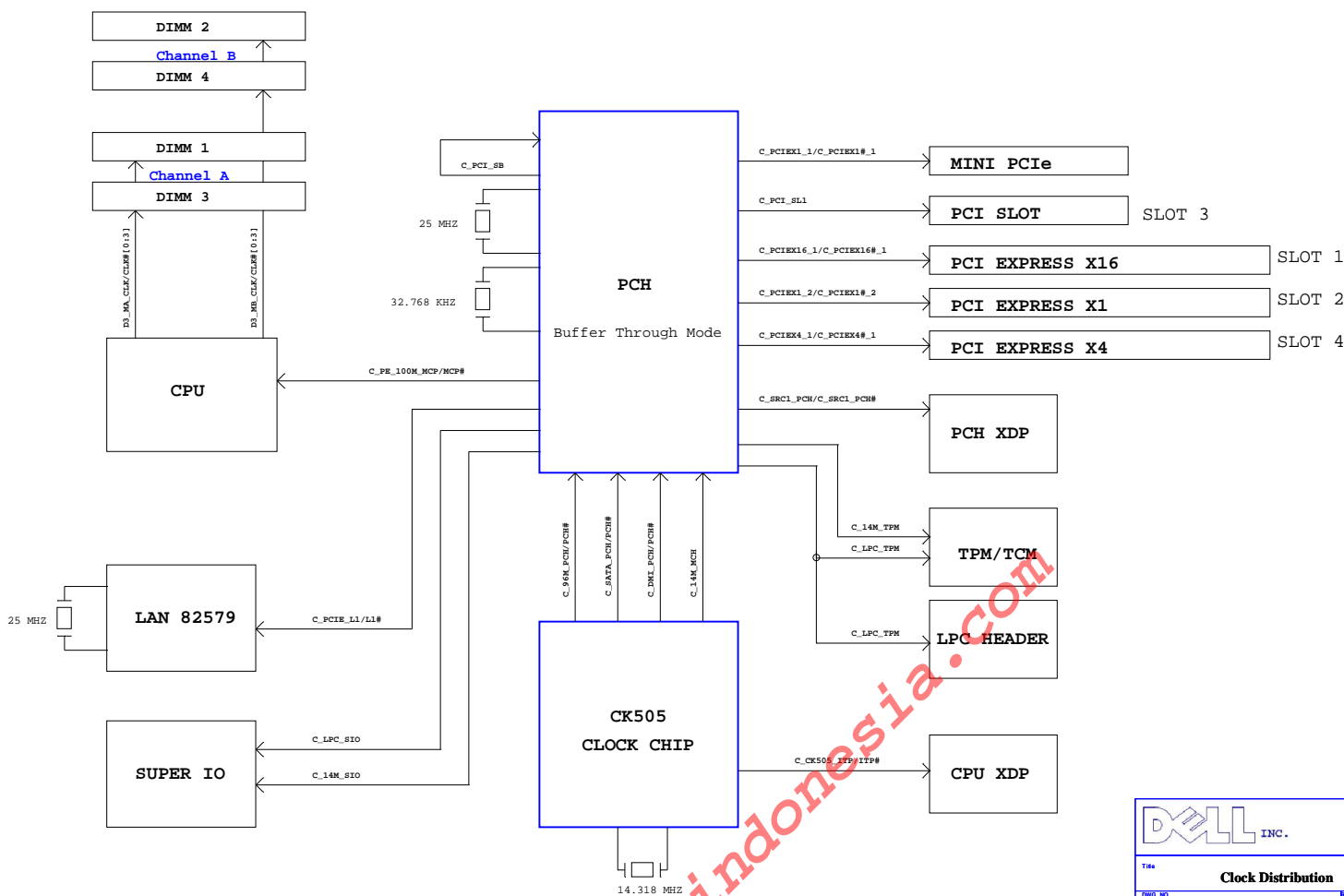
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SMBUS DIAGRAM



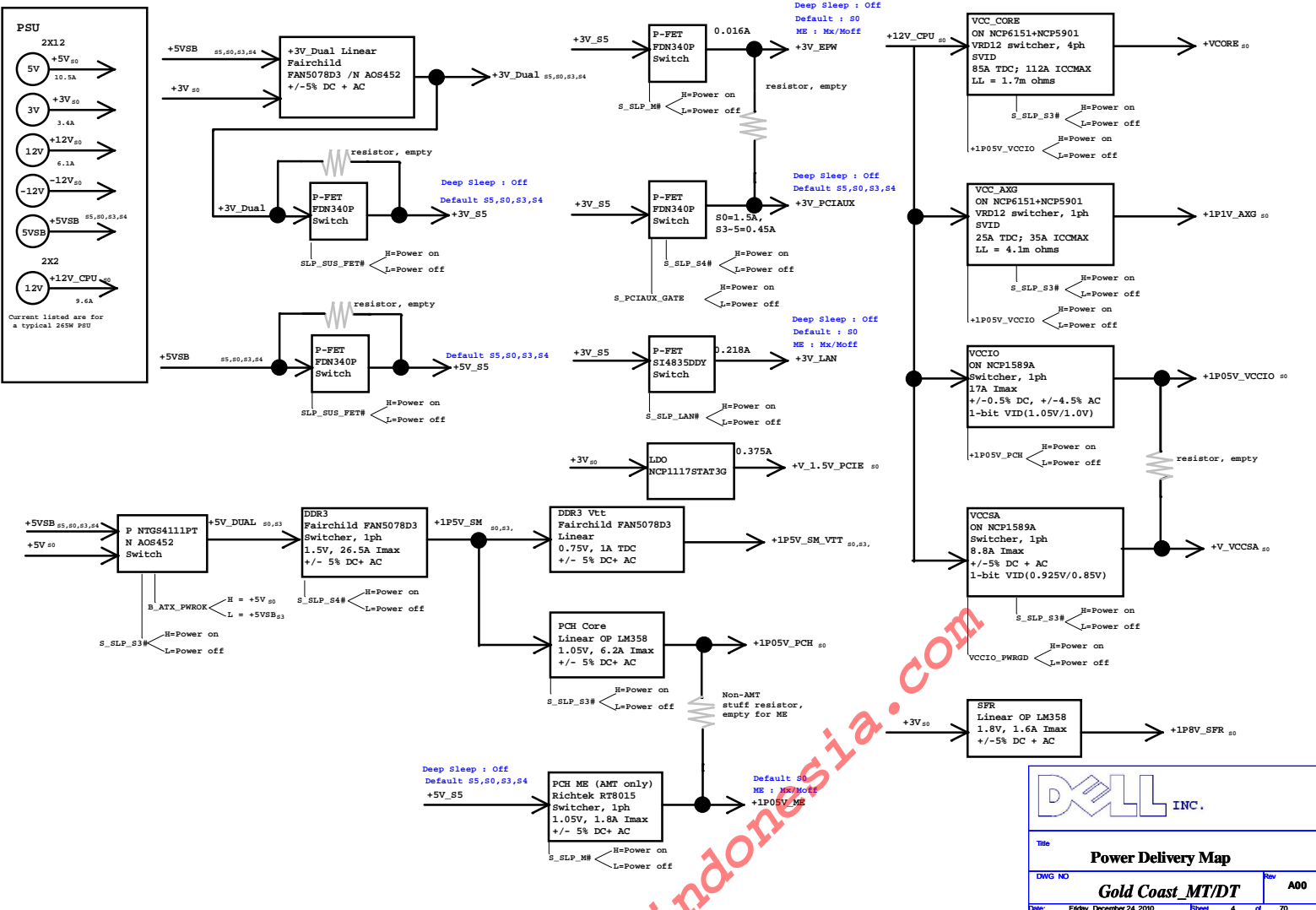
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Title		
Clock Distribution		
DRWG NO	REV	ADD
Gold Coast MT/DT		
DATE	DESIGNED BY	DATE
15th December 2019		

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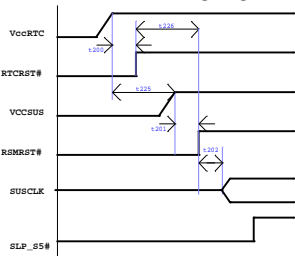
POWER DELIVERY MAP



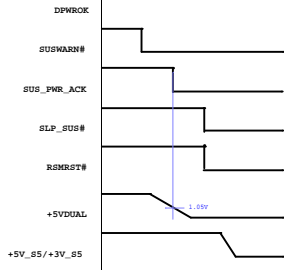
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POWER ON Timing Diagram

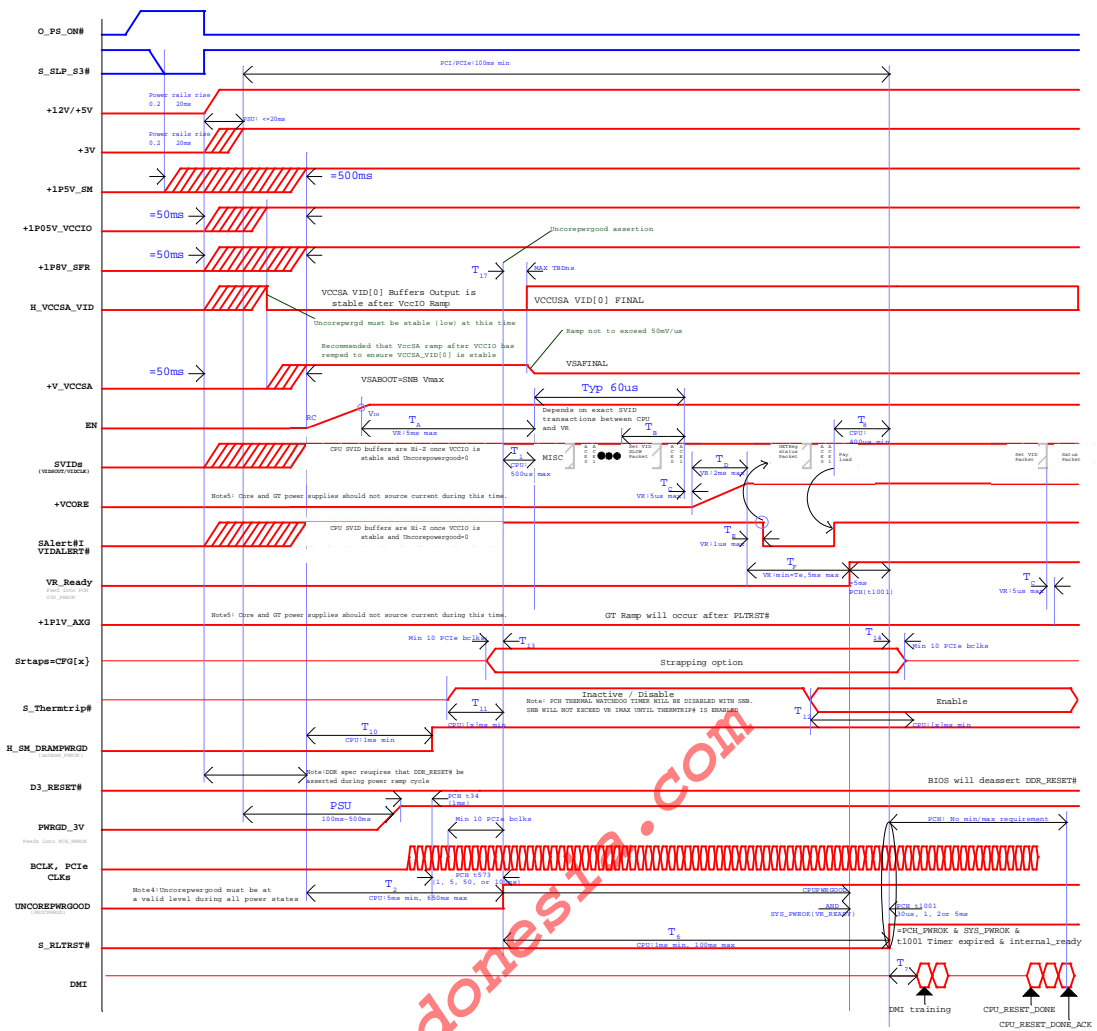
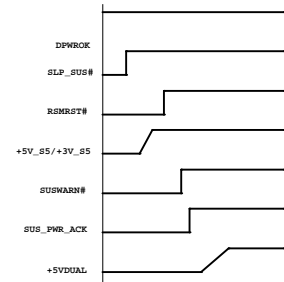
G3 to S4/S5 Timing Diagram



Deep Sleep Entry



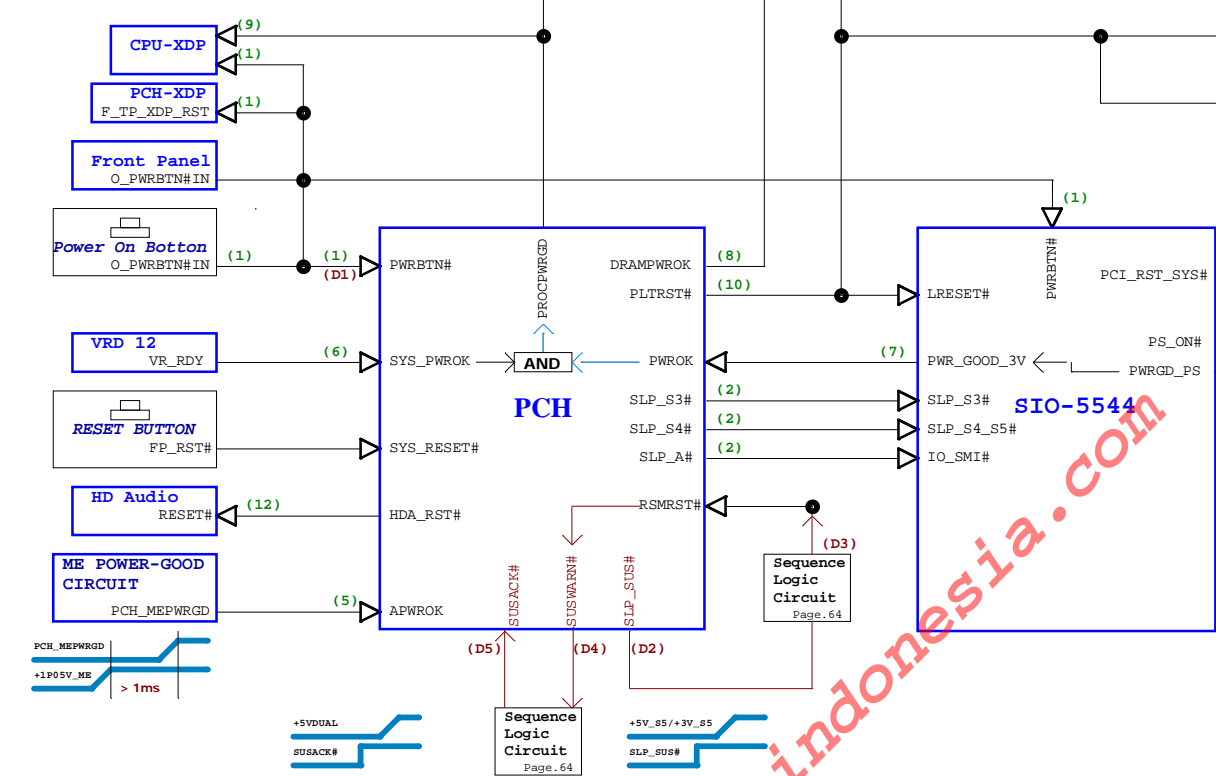
Deep Sleep Exit



RESET / Power Good MAP

Sequence Signal Name:

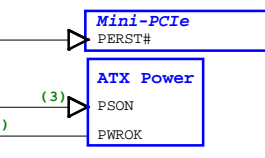
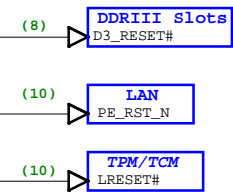
- (1) O_PWRBTN#IN
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PSON#
- (4) B_ATX_PWROK
- (5) PCH_MEPWRGD
- (6) S_PCH_SYSPWROK P_VR_READY
- (7) PWRGD_3V
- (8) H_DRAMPWROK D3_RESET#
- (9) H_PWRGD
- (10) S_PLTRST# H_RESET#_R S_PLTRST#_R
- (11) X_PLTRST#_PCIE_SLOT# K_PCIRST#_SLOT
- (12) A_Z_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O_PWRBTN#IN
- (D2) S_SLP_SUS#
- (D3) S_RSMRST#
- (D4) S_SUSWRN#
- (D5) S_SUS_PWR_ACK#



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Reset / Power Good Map			
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IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot3	C	D	A	B	18	0	0

STRAPPING Table

CFG{17:0}	Description	
{2}	PCI Express static x16 lane numbering reversal	1: normal 0: lane numbers reversed Default
{6:5}	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

Clock Gen.

FREQ	C_CK_BSEL0	C_CK_BSEL1	C_CK_BSEL2
100	1	0	1
133	1	0	0

Default

PIN NAME	NET	Strapping description	
PCI2/TME (PIN4)	C_CK505_33M_PCI2	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI4/SRC5_EN (PIN6)	C_CK505_33M_PCI4	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCIF5/ITP_EN (PIN7)	C_CK505_33M_PCI5	1	CPU_ITP DEFAULT
		0	SRC8
PCI3/CPGP (PIN5)	C_CK505_33M_PCI3	Low	See CFG Table DEFAULT
		Mid	(Set SATA and SRC come from PLL4) See CFG Table
		High	See CFG Table

SIO SMSC5544

PIN NAME	NET	Strapping description	
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#_R	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description
High	1.5V
Low	1.8V

DEFAULT

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

DEFAULT

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable

DEFAULT

No Reboot Mode

SPWR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

DEFAULT

Integrated 1.05V VRM

INTVRMEN	Description
High	Integrated 1.05V VRM: Enable
Low	Integrated 1.05V VRM: Disable

DEFAULT

TLS Confidentiality

GPIO15 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

DEFAULT

Flash Descriptor Override Strap

HDA_SDO	Description
High	Flash descriptor security will be override
Low	Disable ME in Manufacturing Mode

DEFAULT

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description
Low	DMI RX Termination Voltage

DEFAULT

DMI Termination Voltage

NV_CLE (IN-PU)	Description
High	DMI and FDI Tx/Rx Termination Voltage

DEFAULT

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
Low	High	Flash cycle routed to NAND
High	High	Flash cycle routed to SPI

DEFAULT

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description
High	Enable
Low	Disable

DEFAULT

Digital Port C Strap

DDPC_CTRLDATA	Description
High	Configure Port C
Low	Disable

DEFAULT

Title

GPIO/IRQ/IDSEL Table

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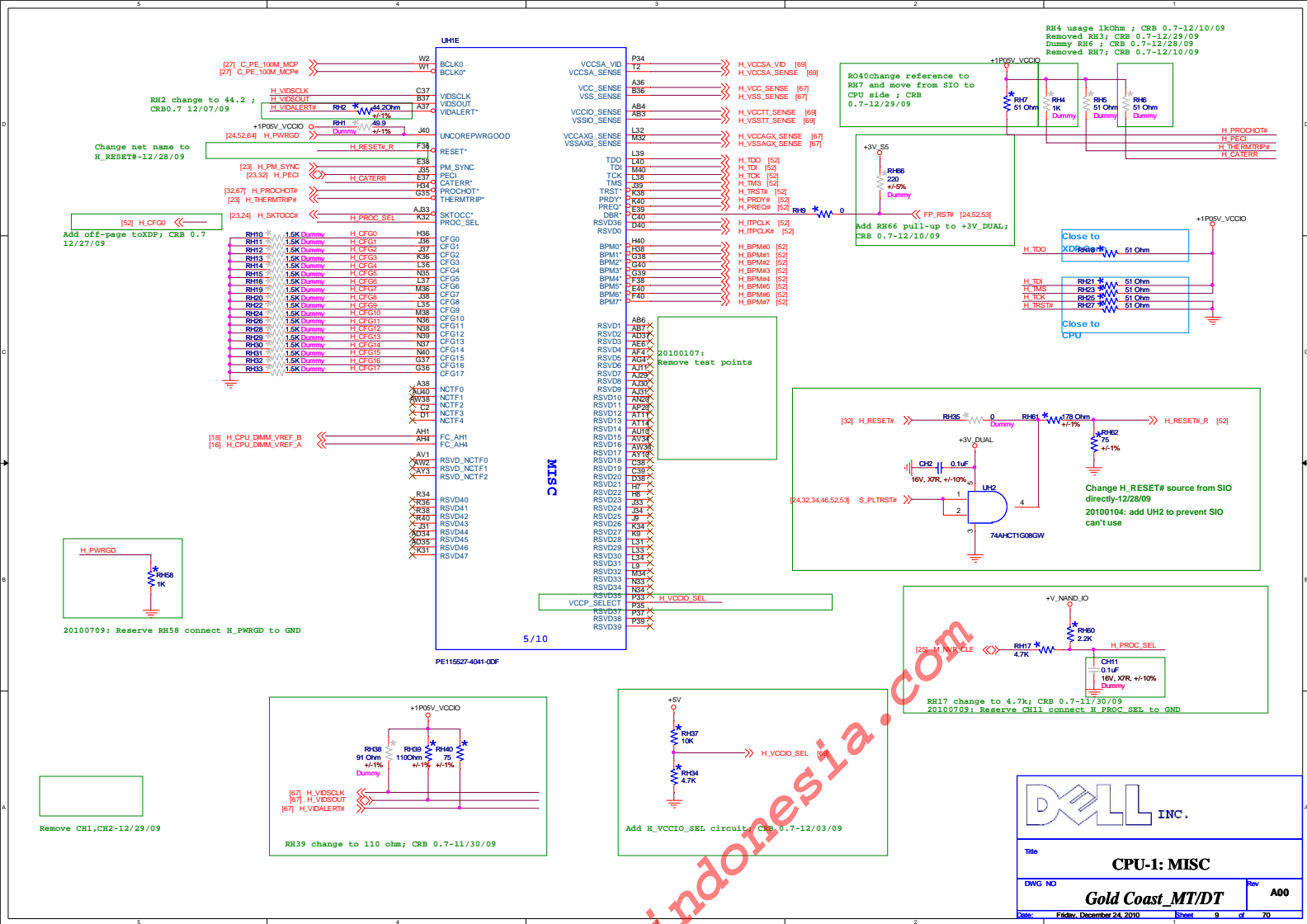
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PCI GPIO Summary							
GPIO	Type	Power Well	Default	IN-PUPD	EX-PUPD	Schematic Usage	
GPIO3	IO	Core	GPI	---	10k pull-up to +3V	S_PECU_RESET#	
GPIO1	IO	Core	GPI	20k IN-PUPD (only on TACH2)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_PL_CHASSIS_ID0	
GPIO2	IO	Core	GPI	---	8.2k pull-up to +3V	PCIE_MINI_CPBUS_DETECT#	
GPIO4	IO	Core	GPI	---	V_DDBP_C_HPD	---	
GPIO4	IO	Core	GPI	---	8.2k pull-up to +3V	V_OPL_VGA_CBL_DET#	
GPIO5	IO	Core	GPI	---	8.2k pull-up to +3V	PCIE_MINI_CPEL_DETECT#	
GPIO6	IO	Core	GPI	20k IN-PUPD (only on TACH2)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_PL_PCH_CBL_DET#	
GPIO7	IO	Core	GPI	20k IN-PUPD (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_PL_PCH_CBL_DET#	
GPIO8	IO	Suspend	GPO	20k IN-PUPD	---	S_TP_PFI#	
GPIO9	IO	Suspend	Native	---	8.2k pull-up to +3V_S5 (dummy)	V_USB_OC_RL_#5	
GPIO10	IO	Suspend	Native	---	10k pull-up to +3V_S5	K_VLAN_PAN#	
GPIO11	IO	Suspend	Native	---	10k pull-up to +3V_S5	M_VAN#	
GPIO12	IO	Suspend	Native	---	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	L_LAN_DISABLE#	
GPIO13	IO	Suspend	GPI	---	10k pull-up to +3V_S5	X1_VAN#	
GPIO14	IO	Suspend	Native	---	10k pull-up to +3V_S5	S_PL_WLON	
GPIO15	IO	Suspend	GPO	20k IN-PUPD	10k pull-up to +3V_S5 (dummy)	S_PCH_GPI5	
GPIO16	IO	Core	GPI	---	10k pull-up to +3V	H_SKTCC_RL_#	
GPIO17	IO	Core	GPI	20k IN-PUPD (only on TACH3)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_PL_CHASSIS_ID1	
GPIO18	IO	Core	GPI	20k IN-PUPD	10k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	S_SATA10P	
GPIO19	IO	Core	Native	---	10k pull-down to GND (dummy)	S_FLIDIRAY_H0F_CBL_DET#	
GPIO20	IO	Core	GPI	---	10k pull-down to GND (dummy)	S_PL_PCH_REV#	
GPIO21	IO	Core	GPI	---	10k pull-up to +3V 4.7k pull-down to GND (dummy)	S_PCH_CONFIG_JUMPER	
GPIO22	IO	Core	Native	20k IN-PUPD	10k pull-up to +3V (dummy)	L_DRO#	
GPIO23	IO	Suspend	GPO	---	100k pull-up to +3V_S5	H_SKTCC#	
GPIO24	IO	Deep Sleep	GPI	20k IN-PUPD	10k pull-up to +3V_DUAL 1k pull-down to GND (dummy)	S_PL_PFI2_F0	
GPIO25	IO	Suspend	GPO	20k IN-PUPD	10k pull-up to +3V_S5 1k pull-down to GND (dummy)	S_PCH_OP28_FU	
GPIO26	IO	Suspend	Native	---	10k pull-up to +3V_S5 (dummy)	S_SLP_LAN#	
GPIO27	IO	Suspend	Native	---	10k pull-up to +3V_DUAL (dummy) 1k pull-down to GND (dummy)	S_SUSVWAKE#	
GPIO28	IO	Deep Sleep	GPI	10k IN-PUPD	8.2k pull-up to +3V_DUAL	S_PWD_CLR	
GPIO29	IO	Core	GPO	---	10k pull-up to +3V (dummy) 220 pull-down to GND	S_PL_BK00	
GPIO30	IO	Core	GPO	---	---	---	
GPIO31	IO	Core	GPI	---	10k pull-up to +3V	PCH_OP014	
GPIO32	IO	Core	GPO	---	10k pull-up to +3V (dummy) 220 pull-down to GND	S_PL_SK01	
GPIO33	IO	Core	GPI	20k IN-PUPD	---	S_PCH_GP36	
GPIO34	IO	Core	GPI	20k IN-PUPD	---	S_PCH_GP37	
GPIO35	IO	Core	GPI	---	10k pull-up to +3V (dummy) 10k pull-down to GND	S_PL_CHASSIS_ID2	
GPIO36	IO	Core	GPI	---	10k pull-up to +3V	K_VP_PRES#	
GPIO37	IO	Suspend	Native	---	---	V_USB_OC_RL_#1	

GPIO41	IO	Suspend	Native	---	---	V_USB_OC_RL_#2	
GPIO42	IO	Suspend	Native	---	---	V_USB_OC_RL_#3	
GPIO43	IO	Suspend	Native	---	8.2k pull-up to +3V_S5 (dummy)	V_USB_OC_RL_#4	
GPIO44	IO	Suspend	Native	20k IN-PUPD	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	S_INTRUD_CBL_DET#	
GPIO45	IO	Suspend	Native	---	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	O_COM_SERV2_DET#	
GPIO46	IO	Suspend	Native	20k IN-PUPD	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	S_PL_BRD_REV1	
GPIO48	IO	Core	GPI	---	10k pull-up to +3V	S_OP048_FU	
GPIO49	IO	Core	GPI	---	8.2k pull-up to +3V	TMR_LSHFT	
GPIO50	IO	Core	Native	---	8.2k pull-up to +3V	K_REQ#1	
GPIO51	IO	Core	Native	20k IN-PUPD	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	K_ONTP#1	
GPIO52	IO	Core	Native	---	8.2k pull-up to +3V	K_REQ#2	
GPIO53	IO	Core	Native	20k IN-PUPD	1k pull-down to GND (dummy)	K_ONTP#2	
GPIO54	IO	Core	Native	---	8.2k pull-up to +3V	K_REQ#3	
GPIO55	IO	Core	Native	20k IN-PUPD	1k pull-down to GND (dummy)	K_ONTP#3	
GPIO57	IO	Suspend	GPI	---	10k pull-up to +3V_S5 (dummy) 47k pull-down to GND	S_OP057_F0	
GPIO58	IO	Suspend	Native	---	10k pull-up to +3V_S5	S_SMLINK_CLK	
GPIO59	IO	Suspend	Native	---	---	V_USB_OC_RL_#6	
GPIO60	IO	Suspend	Native	---	2.2k pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#	
GPIO61	IO	Suspend	Native	---	8.2k pull-up to +3V_S5 (dummy)	S_LPC0#	
GPIO62	IO	Suspend	Native	---	---	S_SUSCLK	
GPIO63	IO	Suspend	Native	---	10k pull-up to +3V_S5	S_PCH_AUX_GATE	
GPIO64	IO	Core	Native	20k IN-PUPD	---	S_TP_CLKOUT1LEX0	
GPIO65	IO	Core	Native	20k IN-PUPD	---	O_IAM_SID_R	
GPIO66	IO	Core	Native	20k IN-PUPD	---	S_TP_CLKOUT1LEX2	
GPIO67	IO	Core	Native	20k IN-PUPD	---	O_IAM_TMR_R	
GPIO68	IO	Core	GPI	20k IN-PUPD (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_PL_BRD_REV2	
GPIO69	IO	Core	GPI	20k IN-PUPD (only on TACH4)	10k pull-up to +3V	O_PRT_DET#	
GPIO70	IO	Core	Native	20k IN-PUPD (only on TACH4)	8.2k pull-up to +3V	S_FP_CHAS_DET#	
GPIO71	IO	Core	Native	20k IN-PUPD (only on TACH4)	10k pull-up to +3V	---	
GPIO72	IO	Suspend	Native (Mobile Only)	20k IN-PUPD	10k pull-up to +3V_S5	S_PCH_OP72_FU	
GPIO74	IO	Suspend	Native	---	10k pull-up to +3V_S5	S_MFG_MODE_OR	
GPIO75	IO	Suspend	Native	---	10k pull-up to +3V_S5	S_SMLINK_DATA	

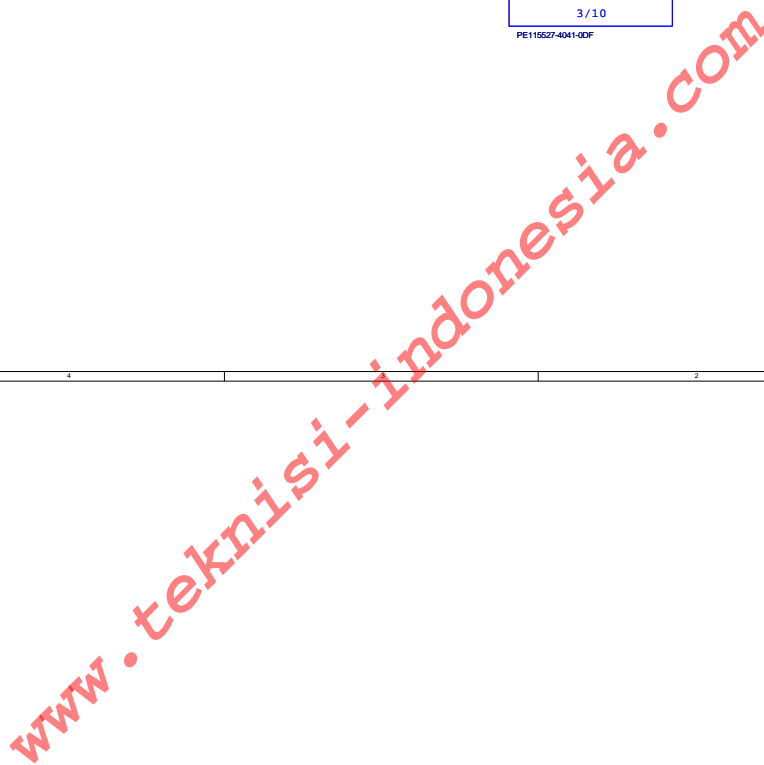
GPIO	PIN NAME	Power well	Buffer Type	EX-PUPD	Signal Name
GPIO0	DWG_LED0# (GPIO0)	VTR	IO	NA	O_DWG_LED#
GPIO1	DWG_LED1# (GPIO1)	VTR	IO	NA	O_DWG_LED#
GPIO2	DWG_LED2# (GPIO2)	VTR	IO	NA	O_DWG_LED#
GPIO3	DWG_LED3# (GPIO3)	VTR	IO	NA	O_DWG_LED#
GPIO4	GPIO4	VTR	IO	NA	NC
GPIO5	H_L_PUPD0# (GPIO5) FREQ_REL# (GPIO5)	VTR	KIOIO	10k pull-up to +3V	O_PIEC_REL#
GPIO6	YELLOW# (GPIO6)	VTR	GND	NA	O_YELLOW#
GPIO7	GREEN# (GPIO7)	VTR	GND	NA	O_GREEN#
GPIO8	SMBUS2 (GPIO8)	VTR	IO	8.2k pull-up to +3V_DUAL (dummy)	S_DRUMH_DATA_R
GPIO9	SMBUS2 (GPIO9)	VTR	IO	8.2k pull-up to +3V_DUAL (dummy)	S_DRUMH_CLK_R
GPIO10	GPIO10	VTR	IO	NA	NC
GPIO13	GPIO13	VTR	IO	NA	NC
GPIO14	(TMR_LSHFT) GPIO14	VTR	IO	8.2k pull-up to +3V	TMR_LSHFT
GPIO15	PWRBTN# (GPIO15)	VTR	IO	10k pull-up to +3V_DUAL	O_PWRBTN#
GPIO16	PROCHOT# (GPIO16) CPU_TEMP# (GPIO16)	VTR	IOIOIO	10k pull-up to +3V_PRES#_VCCIO	O_PROCHOT#
GPIO17	TACH1 (GPIO17)	VTR	IO	10k pull-up to +3V	O_BEN_CPLN#
GPIO18	TACH2 (GPIO18)	VTR	IO	10k pull-up to +3V	O_BEN_CPLN#
GPIO19	TACH3 (GPIO19)	VTR	IO	NA	NC
GPIO20	PWM1 (GPIO20)	VTR	GND	4.7k pull-up to +3V	O_CPUFAN_PWM
GPIO21	PWM2 (GPIO21)	VTR	GND	4.7k pull-up to +3V	O_CPUFAN_PWM
GPIO22	PWM3 (GPIO22)	VTR	GND	4.7k pull-up to +3V	O_CPUFAN_PWM
GPIO23	PWM4 (GPIO23)	VTR	GND	4.7k pull-up to +3V	O_CPUFAN_PWM
GPIO25	GT_CTL_DET# (GPIO25)	VTR	IO	8.2k pull-up to +3V_S5	O_FT_CTL_DET#
GPIO26	PCL_RST_ZVDET# (GPIO26)	VTR	GND	NA	K_PCL_RST_PCE_3L0T#
GPIO27	PCL_RST_ZVDET# (GPIO27)	VTR	GND	NA	H_RESET#
GPIO28	PCL_RST_ZVDET# (GPIO28)	VTR	GND	4.7k pull-up to +500k	O_P3000#
GPIO31	PFC_SMRV_DET# (GPIO31)	VTR	IO	8.2k pull-up to +3V_DUAL	S_SMD_P300V_DET#
GPIO32	GPIO32	VTR	IO	NA	NC
GPIO33	PWR_BTN0_C2# (GPIO33)	VTR	IO	NA	PWR_BTN0_C2#
GPIO34	RMBST0# (GPIO34)	VTR	IO	10k pull-down to GND	O_RMBST0#
GPIO35	GPIO35	VTR	IO	8.2k pull-up to +3V_DUAL	O_BC_3CL
GPIO36	GPIO36 (SMBUS1)	VTR	IOIOIO	8.2k pull-up to +3V_DUAL (dummy)	S_DRUMH_PCL_R
GPIO37	GPIO37 (SMBUS1)	VTR	IOIOIO	8.2k pull-up to +3V_DUAL (dummy)	S_DRUMH_PCL_R
GPIO38	GPIO38 (SMBUS1)	VTR	IOIOIO	8.2k pull-up to +3V_S5	O_V_PNE#
GPIO42	GPIO42 (PHE4)	VTR	IOIO	100k pull-up to +3V_DUAL (dummy)	T_ESTAT_DET#
GPIO43	DCIN1# (GPIO43) DCDET	VTR	IOIO	NA	O_DCIN1_R
GPIO44	DS1# (GPIO44) MCLK	VTR	IO	NA	O_DS1#_R
GPIO45	RSD1 / GPIO45	VTR	IO	NA	O_RSD1_R
GPIO46	RTSR1# (GPIO46)	VTR	GND	NA	O_RTSR1#_R
GPIO47	(V_P3000) GPIO47 (D0)	VTR	IO	NA	O_THD1_S
GPIO48	GPIO48 (SMBUS1)	VTR	IO	NA	O_CTLR1#_R
GPIO49	GPIO49 (SMBUS1)	VTR	IO	8.2k pull-up to +3V_DUAL (dummy)	O_CTLR1#_R
GPIO51	DTTR# (GPIO51) DTTR# (GPIO51)	VTR	IO	8.2k pull-down to GND	O_DTTR1#_R
GPIO52	R11# (GPIO52)	VTR	IO	NA	O_R11#_R
GPIO53	GPIO53 (D0)	VTR	IO	2.2k pull-up to +3V	O_D0#
GPIO54	GPIO54 (D0)	VTR	IO	2.2k pull-up to +3V	O_D0#_R
GPIO55	GPIO55 (D0)	VTR	IO	2.2k pull-up to +3V	O_D0#_R
GPIO56	(PWR2_P300) GPIO56 / RTSR0	VTR	IO	10k pull-up to +3V	O_RTSR0#_R
GPIO57	(V_P300) GPIO57 / D02	VTR	IO	10k pull-up to +3V	O_D02#_R
GPIO58	GPIO58 (D0)	VTR	IO	2.2k pull-up to +3V	O_D0#_R
GPIO59	GPIO59 (D0)	VTR	IO	2.2k pull-up to +3V	O_D0#_R
GPIO61	SMD_RST_P0 (GPIO61) DTTR0#	VTR	IO	8.2k pull-up to +3V	O_DTTR0#_R
GPIO62	GPIO62 (D0)	VTR	IO	2.2k pull-up to +3V	O_D0#_R
GPIO63	R11# (GPIO63)	VTR	IO	10k pull-up to +3V	O_R11#_R
GPIO64	GPIO64 (D0)	VTR	IO	10k pull-up to +3V	O_D0#_R
GPIO65	S1# (GPIO65)	VTR	IO	10k pull-up to +3V	O_S1#_R
GPIO66	S1# (GPIO66)	VTR	IO	10k pull-up to +3V	O_S1#_R
GPIO67	PWR0# (GPIO67)	VTR	IO	10k pull-up to +3V	O_PWR0#_R
GPIO68	SPEAKER (GPIO68) (D0)	VTR	IO	8.2k pull-up to +3V_DUAL (dummy)	O_SPEAKER
GPIO70	(S1P_SMD_P0) GPIO70	VTR	IO	8.2k pull-down to GND	O_S1P_P0#
GPIO72	PCL_READY (V_PNE4) D01 / GPIO72	VTR	IO	10k pull-up to +100k_VCCIO (garbage)	H_PCL_R
GPIO73	PCL_READY (V_PNE4) D01 / GPIO73	VTR	IO	10k pull-up to +100k_VCCIO	O_P30T_P0#

**CPU-1: MISC**

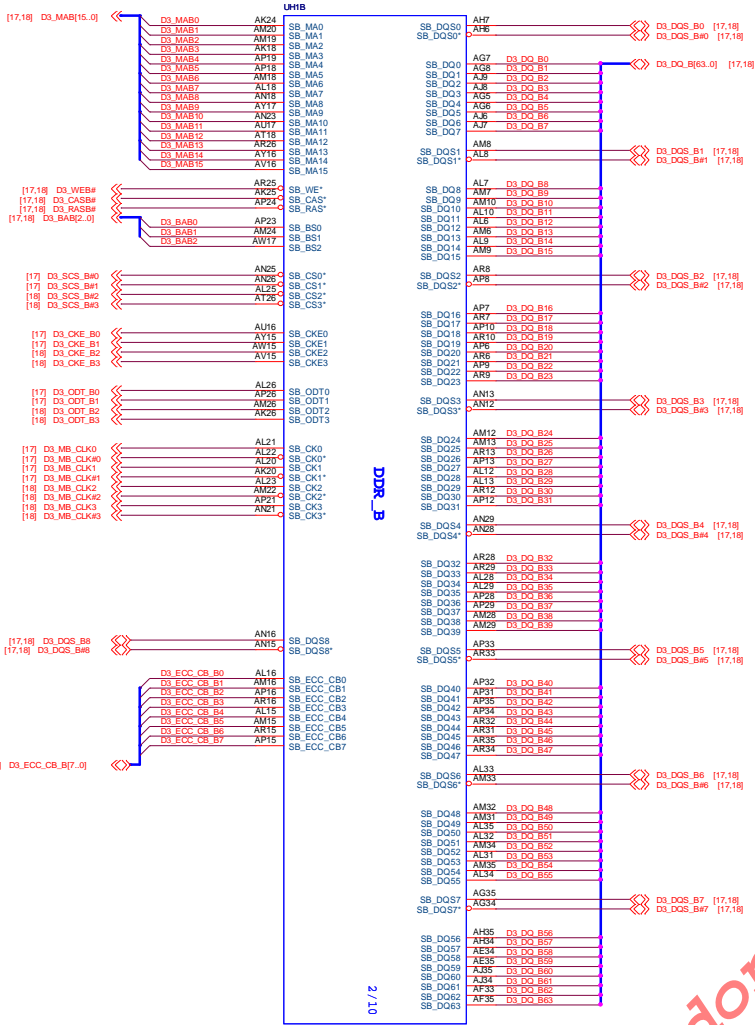
DWG NO	
--------	--

DWG NO **Gold Coast MT/DT**

Gold Coast_MT/DT



Title		CPU-2: FDI/PCIe/DMI	
DWG NO	<i>Gold Coast_MT/DT</i>		Rev
Date:	Friday, December 24, 2010	Sheet	10 of 20



INC.

Title

CPU-4: DDR3_CHB

DWG NO

Gold Coast_MT/DT

Rev

A00

Date

Friday, December 24, 2010

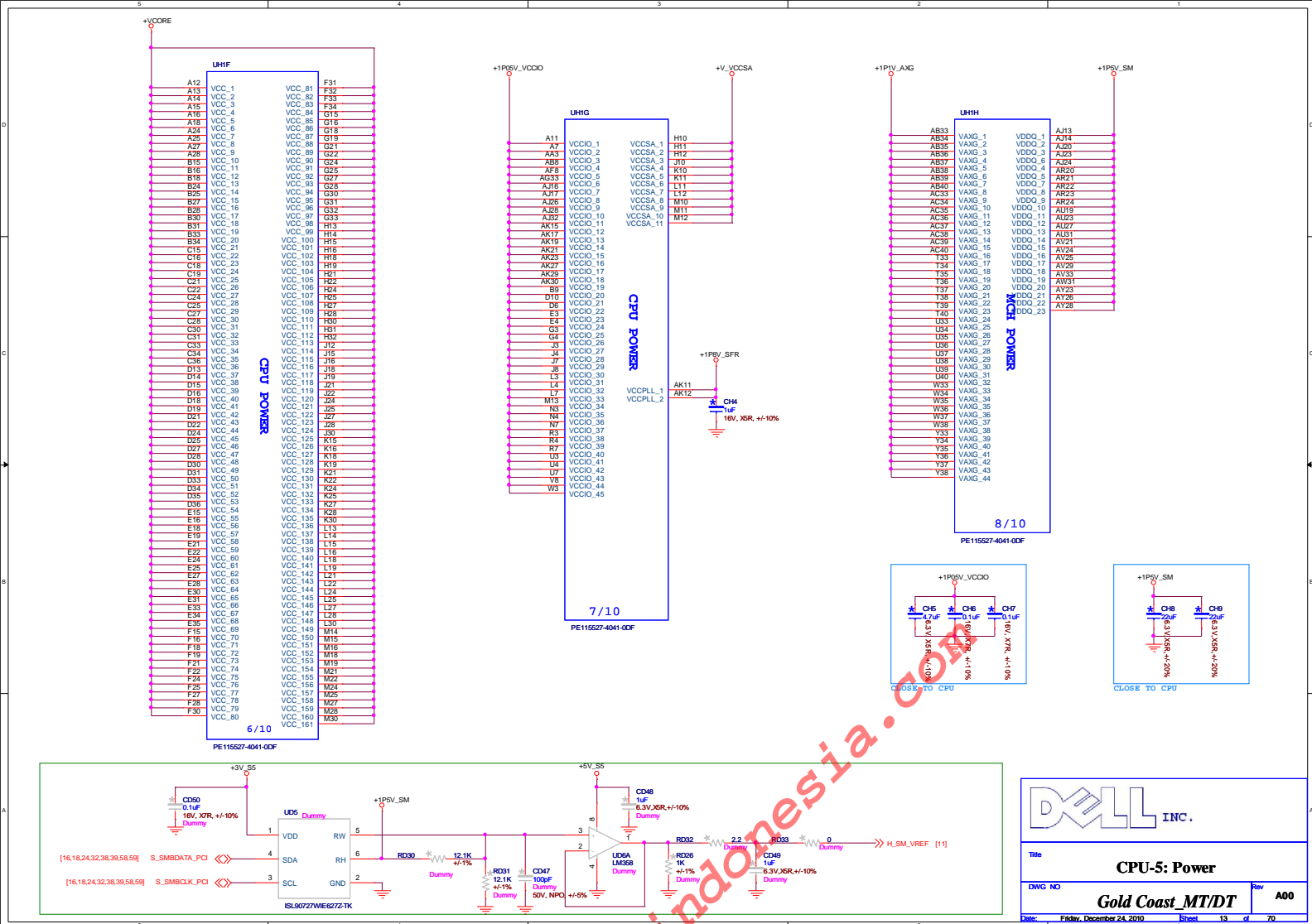
Sheet

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of

20

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UHI1

A17	VSS_1	AM27
A23	VSS_2	AM5
A26	VSS_3	AM30
A29	VSS_4	AM96
A35	VSS_5	AM37
AA33	VSS_6	AM36
AA34	VSS_6	AM39
AA35	VSS_7	AM4
AA36	VSS_8	AM40
AA37	VSS_9	AM5
AA38	VSS_10	AM10
AA6	VSS_11	AM11
AB8	VSS_12	AM14
AC1	VSS_13	AM7
AC6	VSS_14	AM19
AD33	VSS_15	AM2
AD36	VSS_16	AM24
AD38	VSS_17	AM27
AD39	VSS_18	AM30
AD40	VSS_19	AM37
AD5	VSS_20	AM36
AD8	VSS_21	AM39
AE3	VSS_22	AM4
AE33	VSS_23	AM40
AE36	VSS_24	AM5
AF1	VSS_25	AM10
AF34	VSS_26	AM11
AF36	VSS_27	AM14
AF37	VSS_28	AM7
AF40	VSS_29	AM19
AF5	VSS_30	AM2
AF6	VSS_31	AM24
AG36	VSS_32	AM27
AG38	VSS_33	AM30
AG4	VSS_34	AM37
AG2	VSS_35	AM36
AH33	VSS_36	AM39
AH36	VSS_37	AM4
AH37	VSS_38	AM40
AH38	VSS_39	AM5
AH39	VSS_40	AM10
AH40	VSS_41	AM11
AI6	VSS_42	AM14
AI8	VSS_43	AM7
AJ12	VSS_44	AM19
AJ15	VSS_45	AM2
AJ18	VSS_46	AM24
AJ21	VSS_47	AM27
AJ25	VSS_48	AM30
AJ27	VSS_49	AM37
AJ36	VSS_50	AM36
AJ6	VSS_51	AM39
AK1	VSS_52	AM4
AK10	VSS_53	AM40
AK13	VSS_54	AM5
AK14	VSS_55	AM10
AK16	VSS_56	AM11
AK22	VSS_57	AM14
AK28	VSS_58	AM7
AK31	VSS_59	AM19
AK32	VSS_60	AM2
AK33	VSS_61	AM24
AK34	VSS_62	AM27
AK35	VSS_63	AM30
AK36	VSS_64	AM37
AK37	VSS_65	AM36
AK4	VSS_66	AM39
AK40	VSS_67	AM4
AK5	VSS_68	AM40
AK6	VSS_69	AM5
AK7	VSS_70	AM10
AK8	VSS_71	AM11
AK9	VSS_72	AM14
AL11	VSS_73	AM7
AL14	VSS_74	AM19
AL17	VSS_75	AM2
AL19	VSS_76	AM24
AL24	VSS_77	AM27
AL27	VSS_78	AM30
AL30	VSS_79	AM37
AL36	VSS_80	AM36
AL36	VSS_81	AM39
AL5	VSS_82	AM4
AM1	VSS_83	AM40
AM11	VSS_84	AM5
AM14	VSS_85	AM10
AM17	VSS_86	AM11
AM2	VSS_87	AM14
AM21	VSS_88	AM7
AM23	VSS_89	AM19
AM25	VSS_90	AM2

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PE115527-4041-00F

UHIJ

AT6	VSS_171	F37
AT9	VSS_172	F39
AD1	VSS_173	VSS_258
AD5	VSS_174	VSS_259
AD6	VSS_175	VSS_260
AD3	VSS_176	VSS_261
AD4	VSS_177	VSS_262
AD8	VSS_178	VSS_263
AUE	VSS_179	VSS_264
AV10	VSS_180	VSS_265
AV11	VSS_181	VSS_266
AV14	VSS_182	VSS_267
AV17	VSS_183	VSS_268
AV2	VSS_184	VSS_269
AV35	VSS_185	VSS_270
AV36	VSS_186	VSS_271
AV6	VSS_187	VSS_272
AW10	VSS_188	VSS_273
AW11	VSS_189	VSS_274
AW14	VSS_190	VSS_275
AW16	VSS_191	VSS_276
AW36	VSS_192	VSS_277
AW6	VSS_193	VSS_278
AY11	VSS_194	VSS_279
AY14	VSS_195	VSS_280
AY16	VSS_196	VSS_281
AY35	VSS_197	VSS_282
AY4	VSS_198	VSS_283
AY6	VSS_199	VSS_284
AY8	VSS_200	VSS_285
B10	VSS_201	VSS_286
B13	VSS_202	VSS_287
B14	VSS_203	VSS_288
B23	VSS_204	VSS_289
B25	VSS_205	VSS_290
B29	VSS_206	VSS_291
B32	VSS_207	VSS_292
B35	VSS_208	VSS_293
B38	VSS_209	VSS_294
B4	VSS_210	VSS_295
C11	VSS_211	VSS_296
C12	VSS_212	VSS_297
C17	VSS_213	VSS_298
C20	VSS_214	VSS_299
C23	VSS_215	VSS_300
C26	VSS_216	VSS_301
C29	VSS_217	VSS_302
C35	VSS_218	VSS_303
C35	VSS_219	VSS_304
C35	VSS_220	VSS_305
C6	VSS_221	VSS_306
D17	VSS_222	VSS_307
D2	VSS_223	VSS_308
D20	VSS_224	VSS_309
D213	VSS_225	VSS_310
D26	VSS_226	VSS_311
D29	VSS_227	VSS_312
D32	VSS_228	VSS_313
D37	VSS_229	VSS_314
D37	VSS_230	VSS_315
D4	VSS_231	VSS_316
D5	VSS_232	VSS_317
D6	VSS_233	VSS_318
D9	VSS_234	VSS_319
E11	VSS_235	VSS_320
E17	VSS_236	VSS_321
E20	VSS_237	VSS_322
E23	VSS_238	VSS_323
E26	VSS_239	VSS_324
E26	VSS_240	VSS_325
E32	VSS_241	VSS_326
E36	VSS_242	VSS_327
E7	VSS_243	VSS_328
E8	VSS_244	VSS_329
F11	VSS_245	VSS_330
F10	VSS_246	VSS_331
F13	VSS_247	VSS_332
F15	VSS_248	VSS_333
F17	VSS_249	VSS_334
F2	VSS_250	VSS_335
F20	VSS_251	VSS_336
F23	VSS_252	VSS_337
F26	VSS_253	VSS_338
F29	VSS_254	VSS_339
F35	VSS_255	VSS_340
F35	VSS_256	VSS_341
F35	VSS_257	VSS_342
F35	VSS_258	VSS_343
F35	VSS_259	VSS_344
F35	VSS_260	VSS_345
F35	VSS_261	VSS_346
F35	VSS_262	VSS_347
F35	VSS_263	VSS_348
F35	VSS_264	VSS_349
F35	VSS_265	VSS_350
F35	VSS_266	VSS_351
F35	VSS_267	VSS_352
F35	VSS_268	VSS_353
F35	VSS_269	VSS_354
F35	VSS_270	VSS_355
F35	VSS_271	VSS_356
F35	VSS_272	VSS_357
F35	VSS_273	VSS_358
F35	VSS_274	VSS_359
F35	VSS_275	VSS_360

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PE115527-4041-00F

B39 update to RSVD48;
PDG 0.7-12/07/09

ED6: B39 defined "VSS_NCTF"
CRB: B39 defined "RSVD"
Pin B39 follow CRB pin define;
CRB 0.7-12/10/09

TPH65

B39

RSVD48

VSS_NCTF#2

AY37

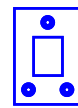
VSS_NCTF4

B3

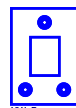
VSS_NCTF5



UHI_1



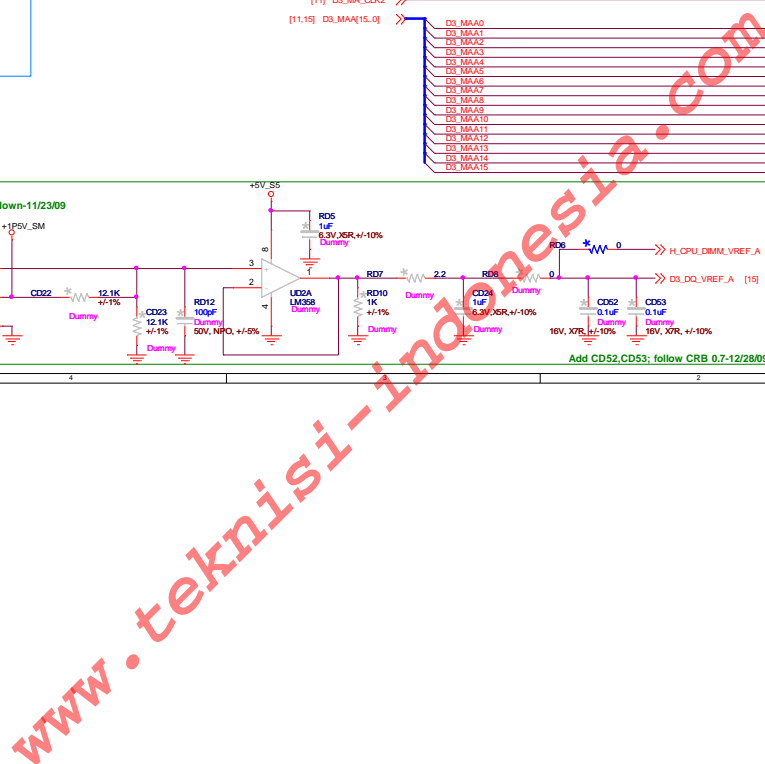
Backplate



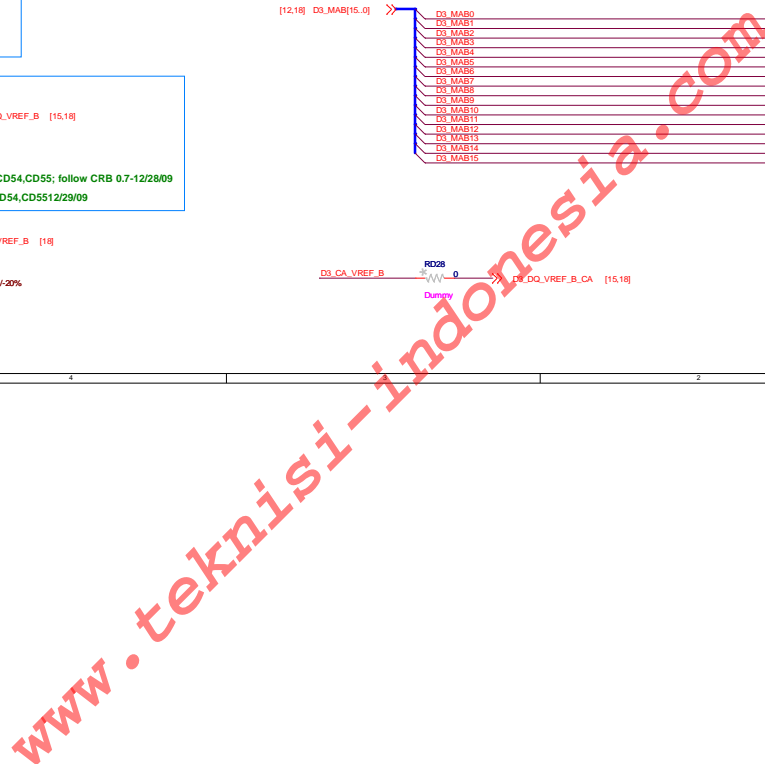
UHI_B Backplate

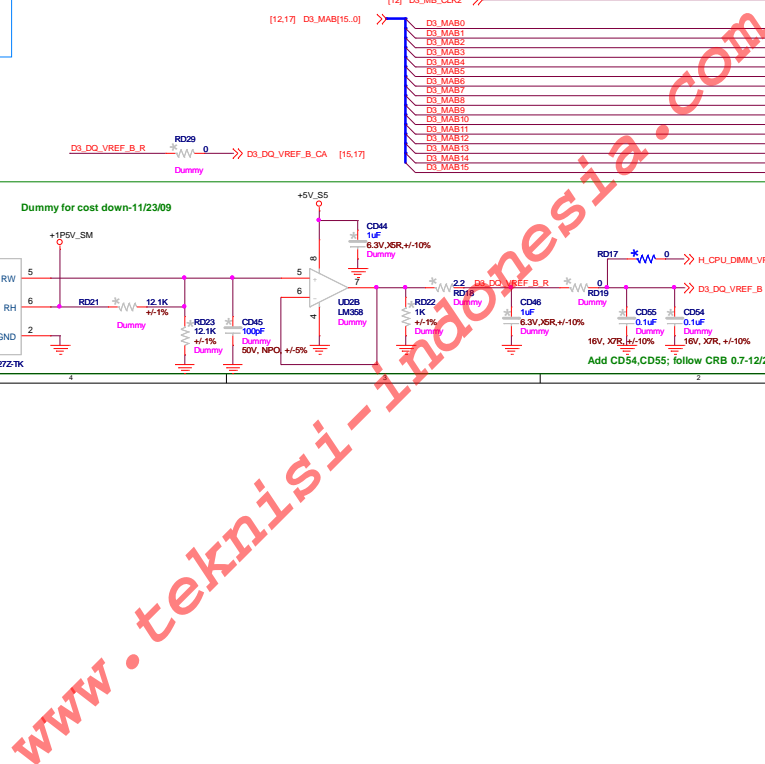


Title		CPU-6: GND	
DWG NO	Gold Coast_MT/DT		Rev A00
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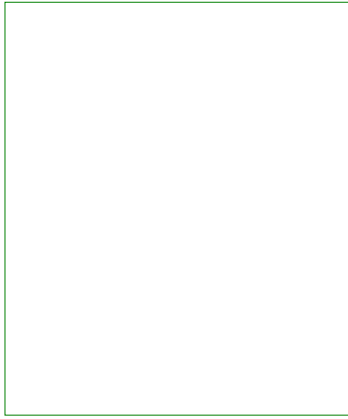


D3_ECC_CB_B[7..0] [12:18]



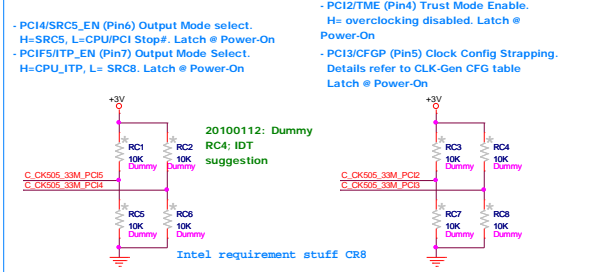
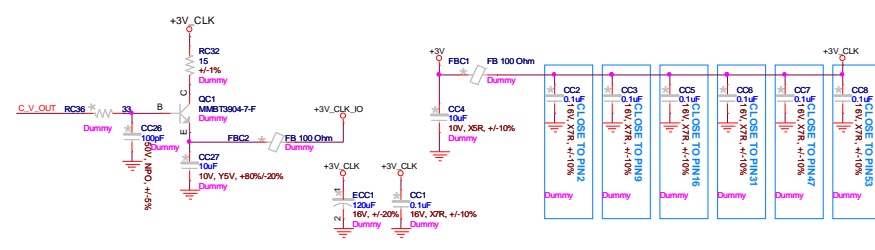


20100106: Remove ONFI function since not support



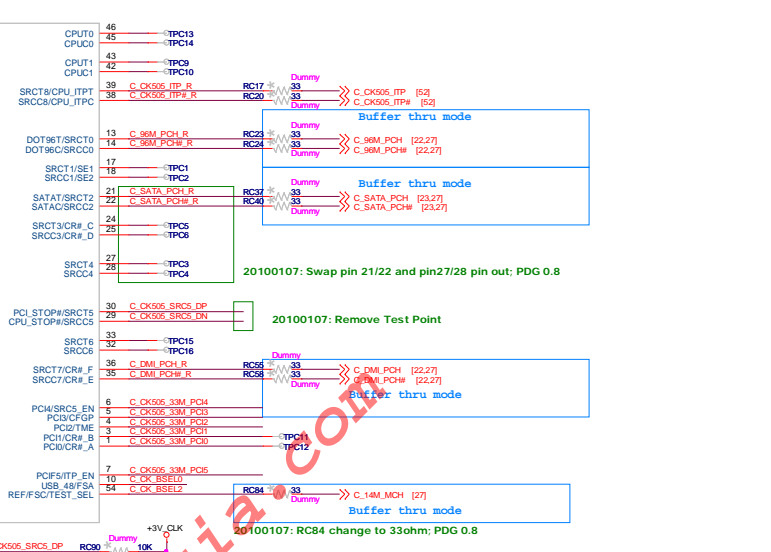
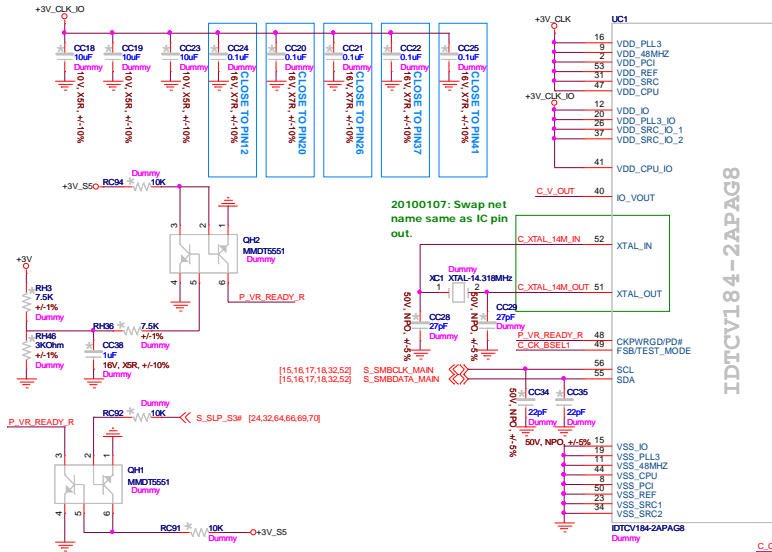
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Title	
TBD	
DWG NO	Rev
Gold Coast_MT/DT	
A00	
Date	Sheet
Friday, December 24, 2010	19 of 20

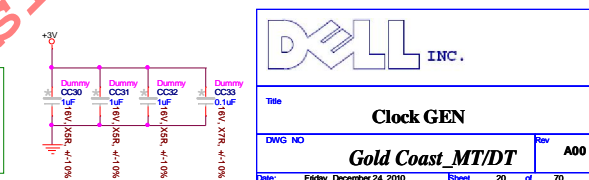
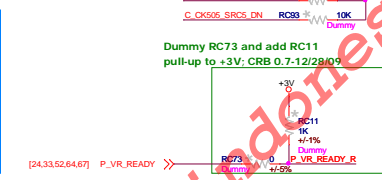


+3V_CLK_IO

Dummy CK505 circuit for Cost down
Add CK505 buffer thru mode circuit-20091225



FRBQ	BSEL0	BSEL1	BSEL2
1.00	1	0	1
1.33	1	0	0

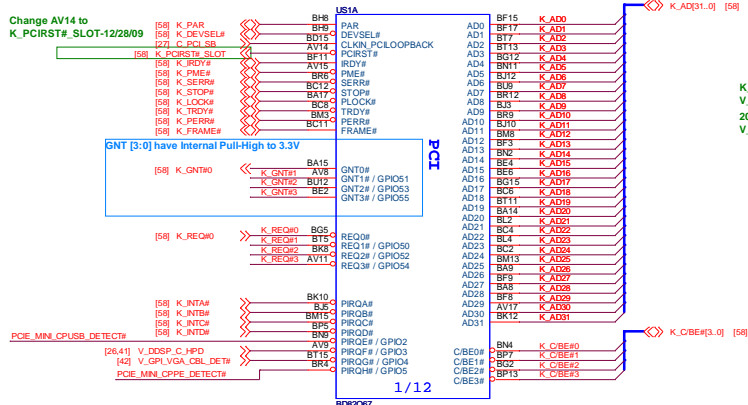


Clock GEN

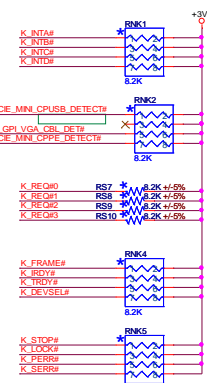
DWG NO: **Gold Coast_MT/DT** Rev: **A00**

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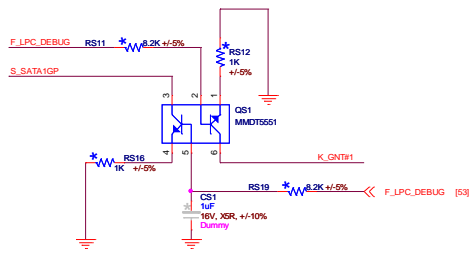
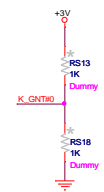
Change AV14 to
K_PCIRST#_SLOT-12/28/09



K_INTF# change to
V_DDSP_C_HPDI-12/28/09
20100108: Remove
V_DDSP_C_HPDI pull-up



K_PME# add RS198 to pull-up
+3V_PCH_AUX; CRB 0.7-12/28/09
20100108: Dummy RS198;
PDG 0.8



S_SATA1GP has external 10k pull-up; CRB 0.7

20091209: Have to check with Intel
20091230: Reserved RS171 and
RS201 for Boot select

Boot BIOS Select

Boot Device	GNT1	SATA1GP
LPC	0	0
PCI	1	0
NAND	0	1
SPI	1	1

[23] S_SATA1GP

GNT3# Internal pull-up.

K_GNT2 RS15 1K
K_GNT3 RS17 4.7K

DG 0.7
GNT3 is top block swap mode:
connect to ground with 4.7k ohm weak
pull down resistor for top block swap mode
GNT2#/GPIO3:ESI strap for server platform
ONLY Do not pull low.

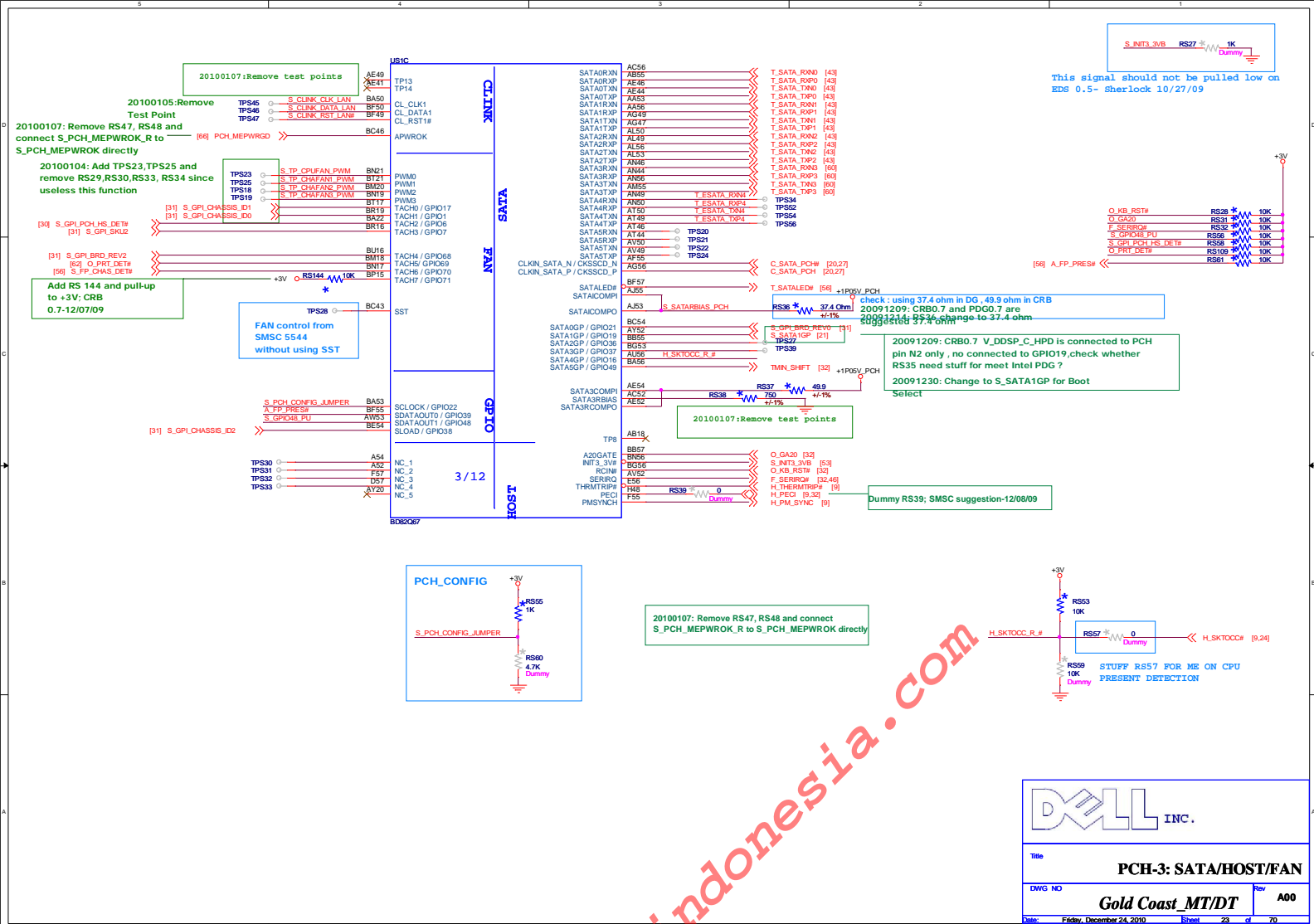
DELL INC.

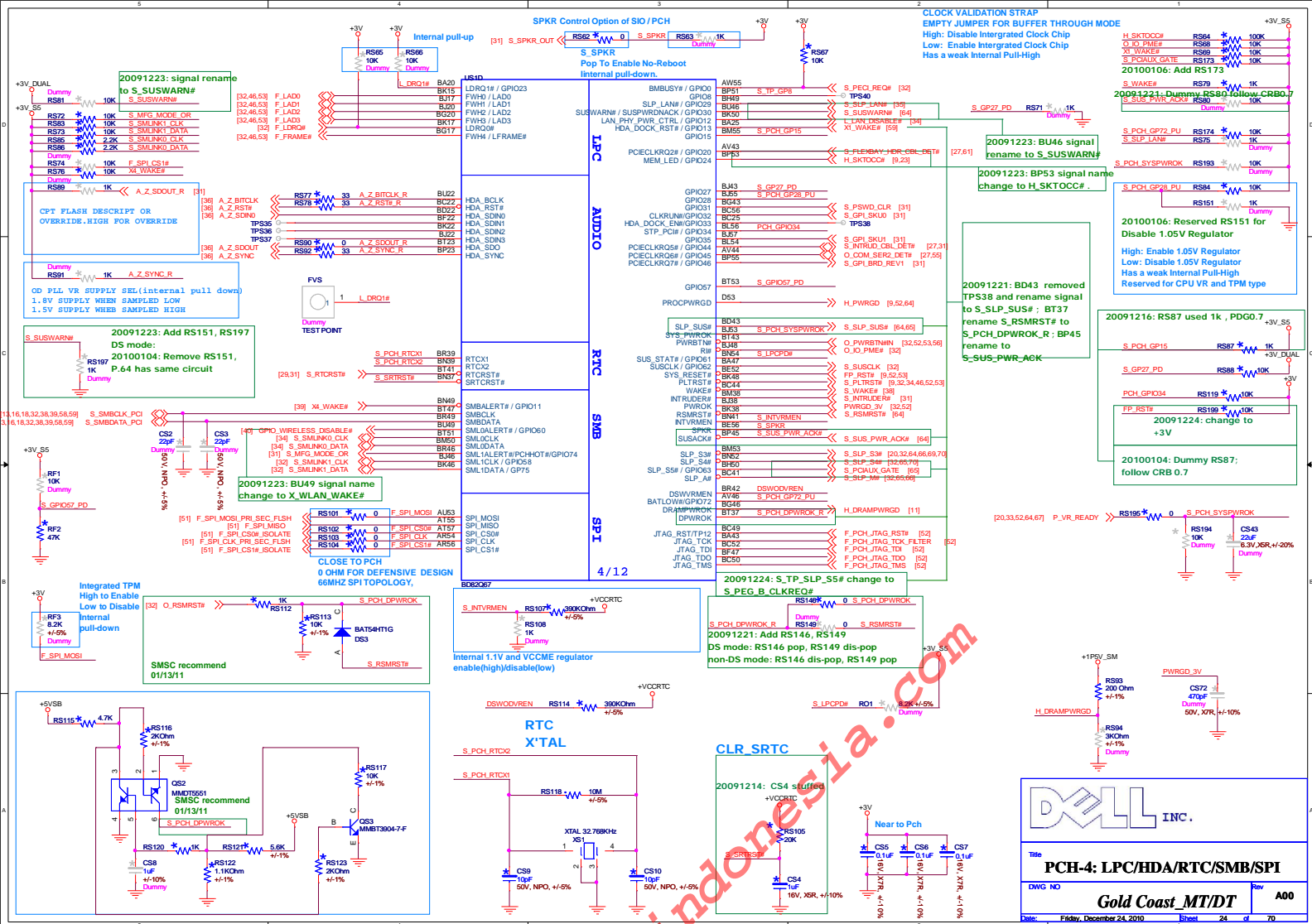
Title: **PCH-1: PCI**

DWG NO: **Gold Coast_MT/DT** Rev: **A00**

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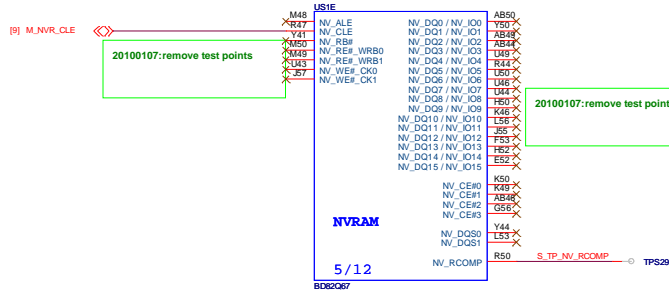
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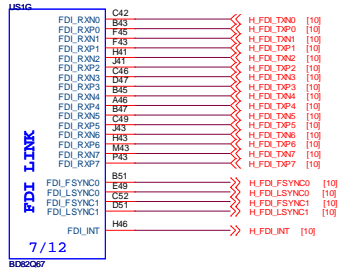


20100106: Remove ONFI function since not support

S_NVR_CLE internal pull-down.



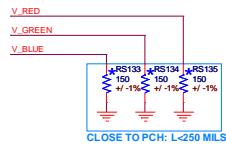
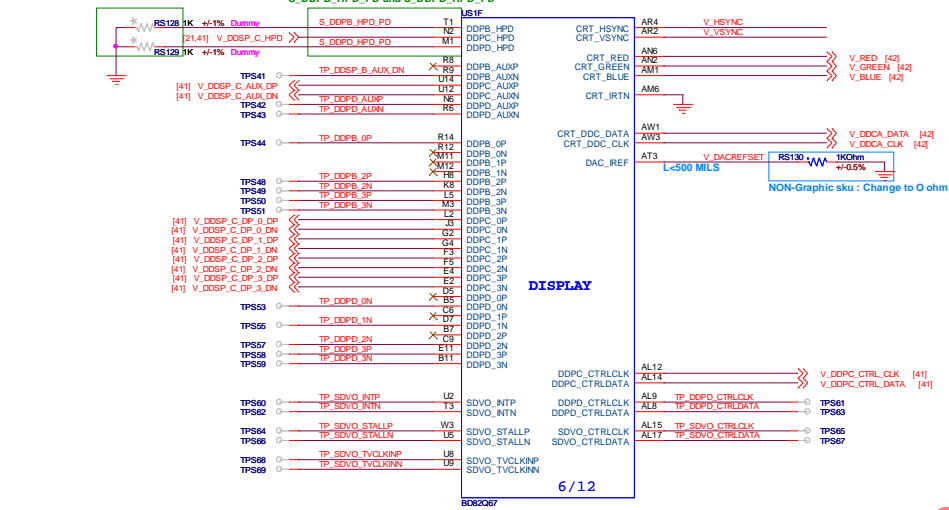
20100107:remove test points



 INC.	
Title	
PCH-57: NVRAM/FDI	
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20100108: Dummy RS128,RS129: CRB 0.7

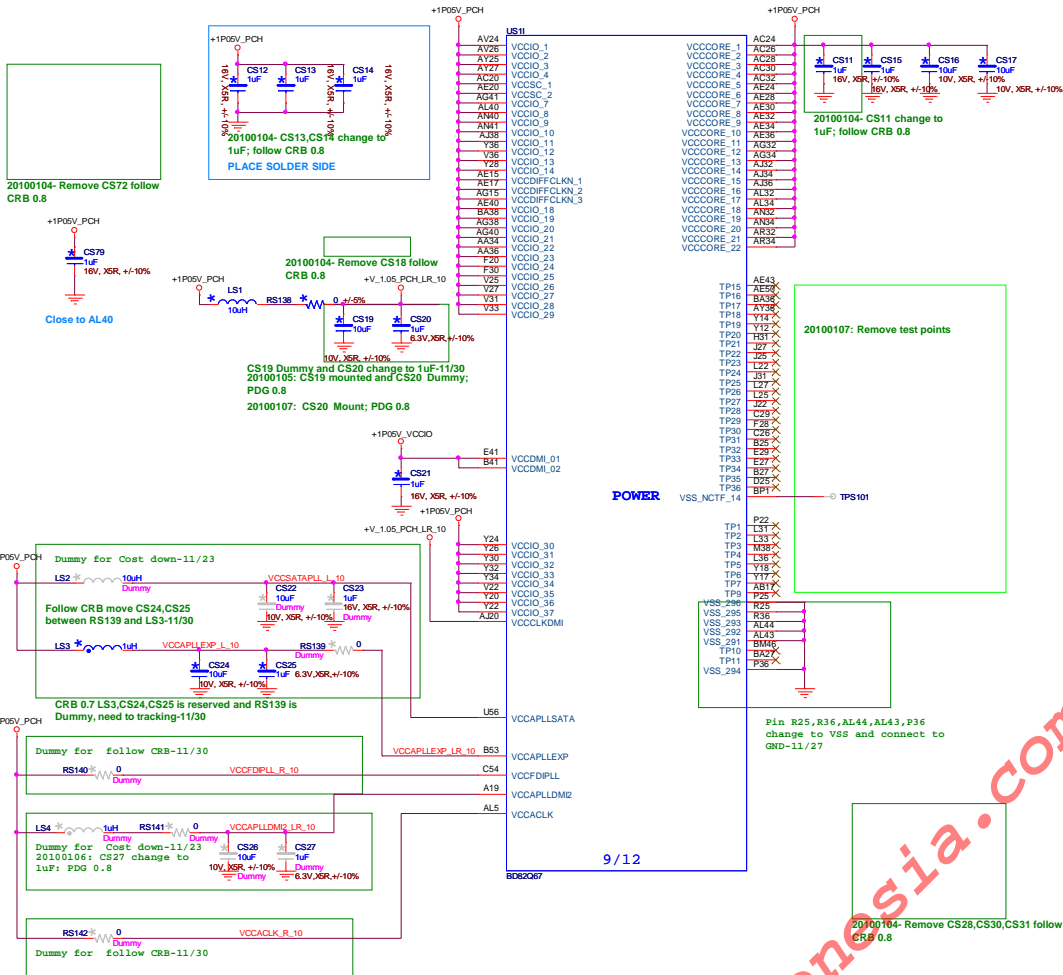
20100107: Correct pin T1 and M1 net name to S_DDPB_HPD_PD and S_DDPD_HPD_PD



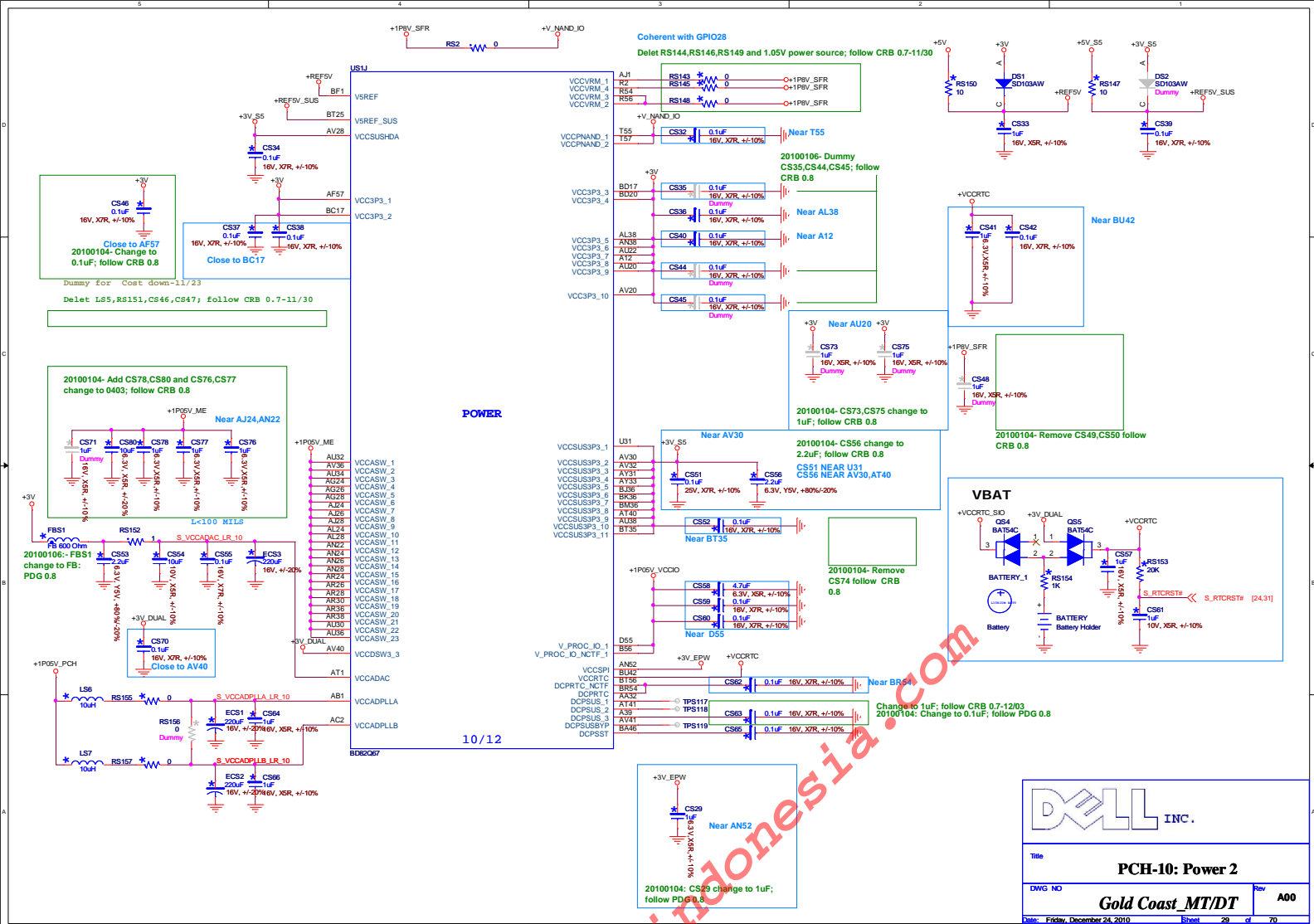
NON-Graphic sku : Change to 0 ohm

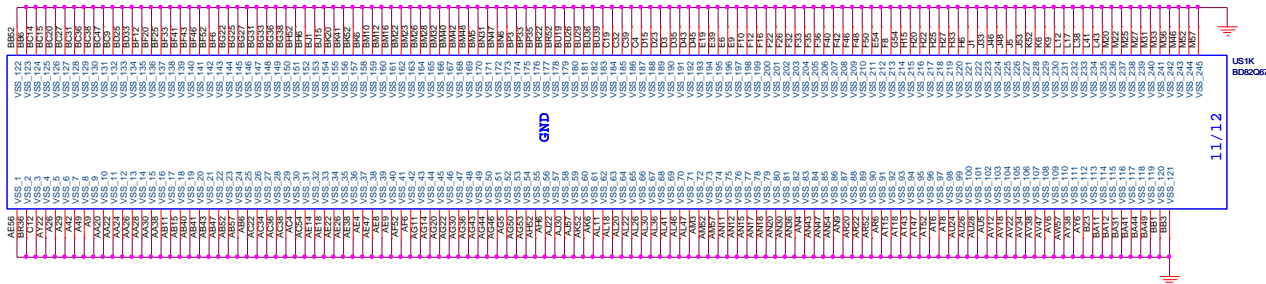


DELL INC.	
Title PCH-6: Display	
DWG NO	Rev A00
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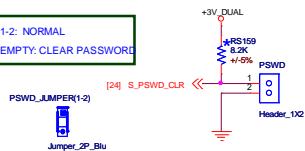
INC.		
Title		
PCH-9: Power 1		
DWG NO	Rev	A00
Gold Coast_MT/DT		
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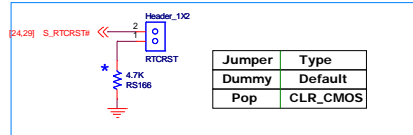


Clear Password

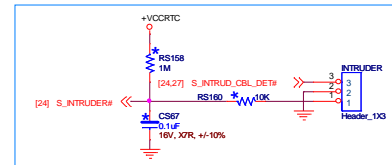
1-2: NORMAL
EMPTY.CLEAR PASSWORD



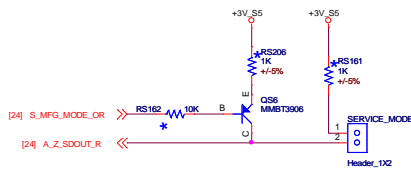
CLR_CMOS



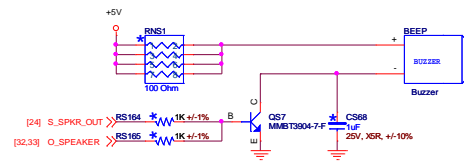
Chassis Intruder



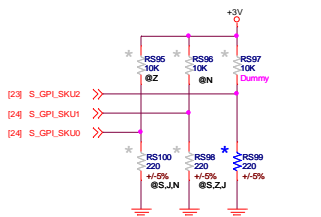
SERVICE_MODE



BEEP



SKU ID



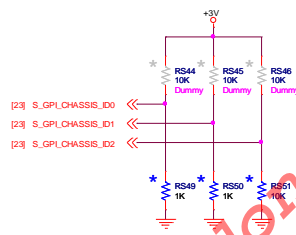
SKU ID

SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	non TPM/TCM
1	1	Reserved

Chassis ID

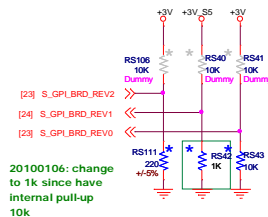
check : need to update table

ID2	ID1	ID0	Type
1	0	1	SFF
1	0	0	Tambor
0	0	0	MT/DT
0	1	1	USFF

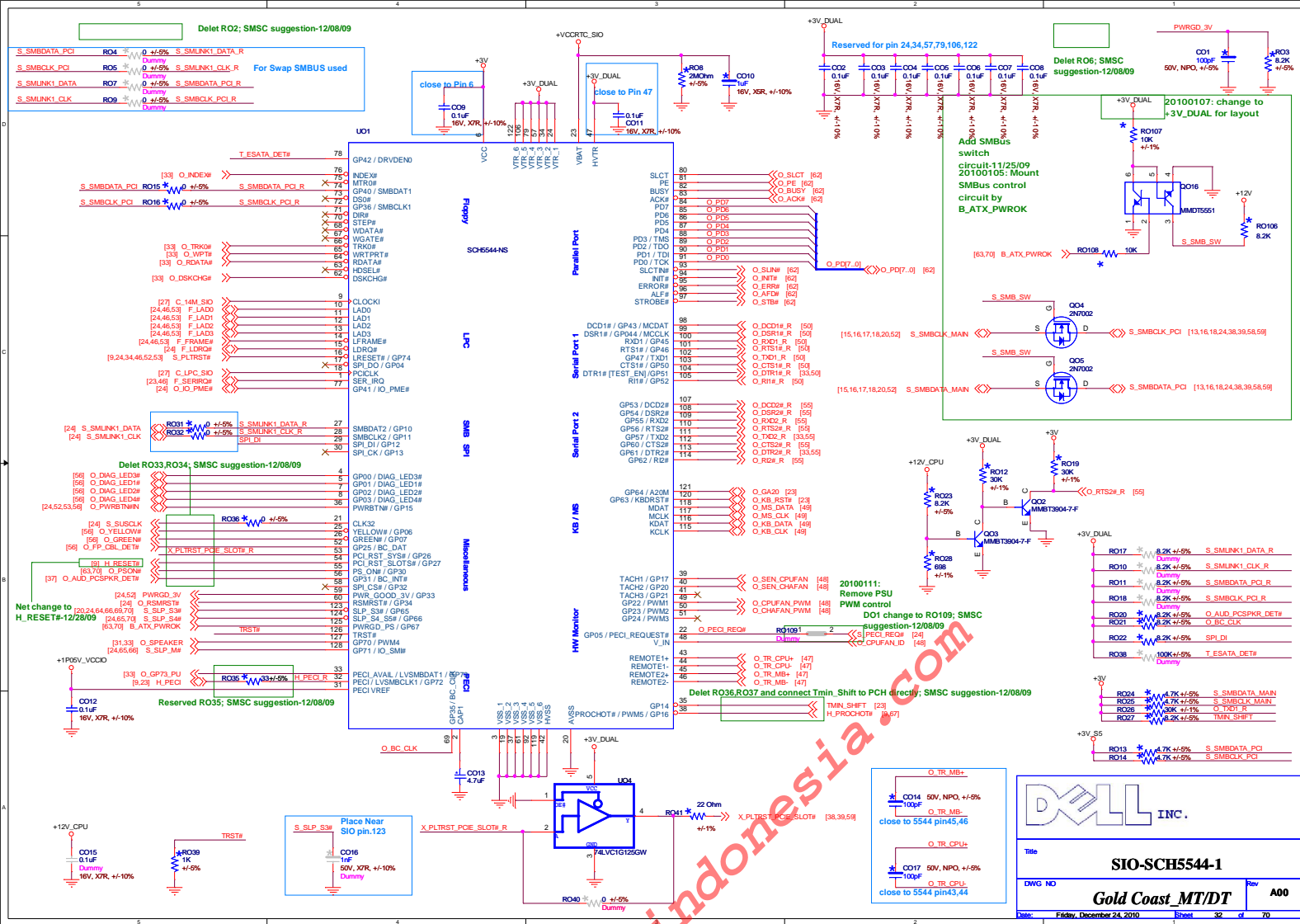


Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

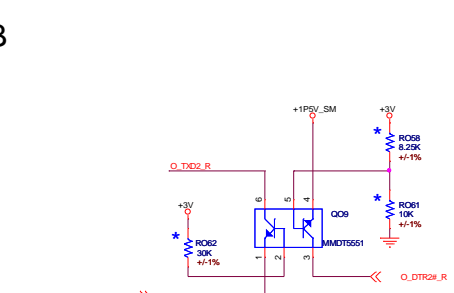
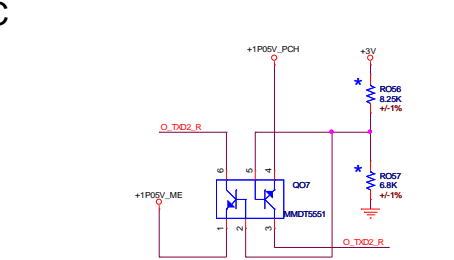
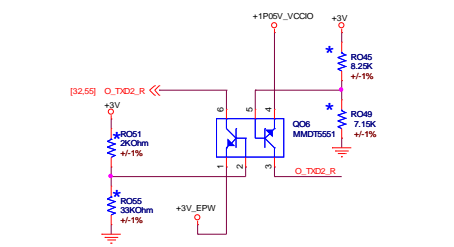
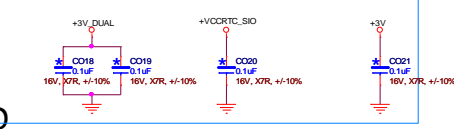
BOARD ID



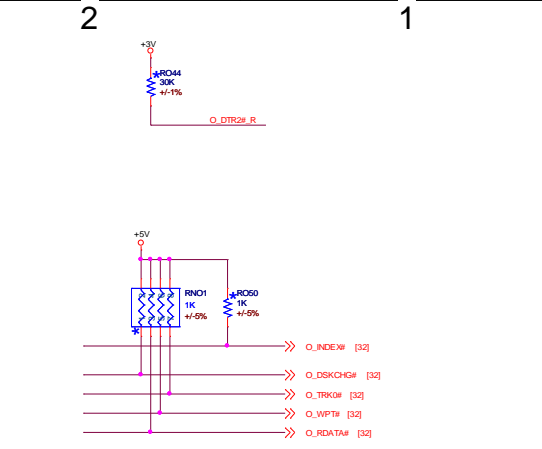
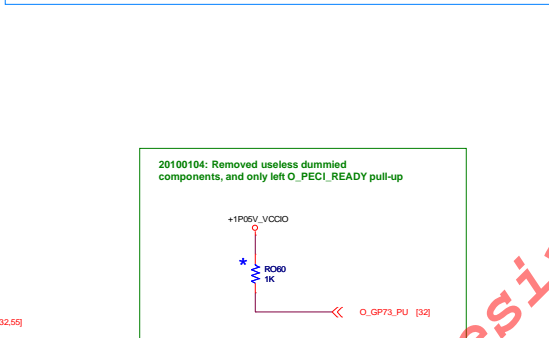
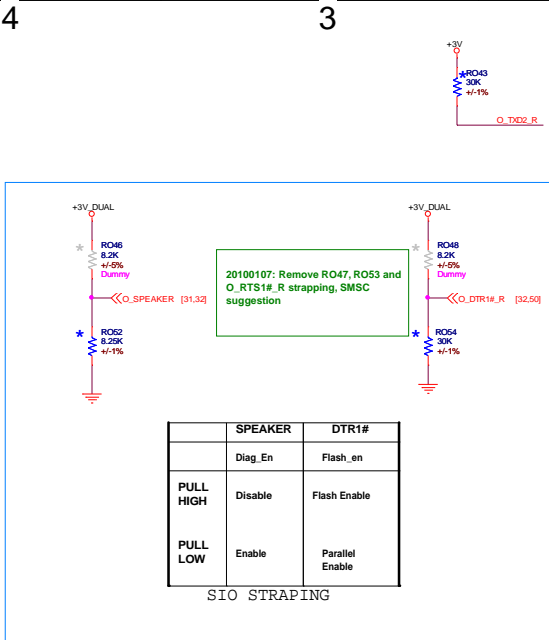
PCH MISC Conn/BUZ/ID	
DWG NO	Rev
Gold Coast_MT/DT	A00
Date: Friday, December 24, 2010	Sheet 31 of 70



SCH5544 Decoupling



5544 PRE-POST DIAG PG GENERATION



DELL INC.

Title: **SIO-SCH5544-2 (MISC)**

DWG NO: **Gold Coast MT/DT** Rev: **A00**

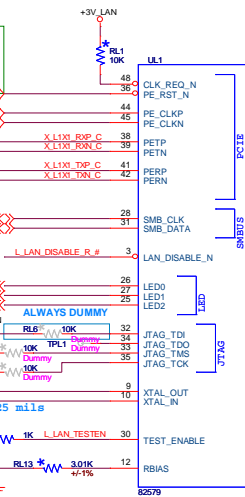
Date: Friday, December 24, 2010 Sheet: 33 of 70

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20091216 Intel 82579 schematic check list 0.5:
Change net name from CLK_REQ_N to S_FLEXBAY_HDR_CBL_DET#
20100105: Remove RL2 and S_FLEXBAY_HDR_CBL_DET#
connection since useless; PDG 0.8

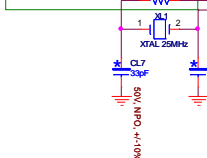
near the PCIe transmitter:
[22] X.L1XI_R0P << CL1 10.1uF
[22] X.L1XI_R0N << CL3 10.1uF
[22] X.L1XI_T0P << CL2 10.1uF
[22] X.L1XI_T0N << CL4 10.1uF

[24] S_SMLINK0_CLK
[24] S_SMLINK0_DATA

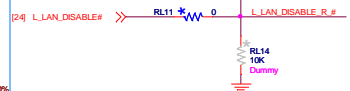
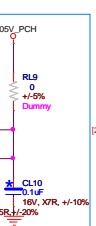
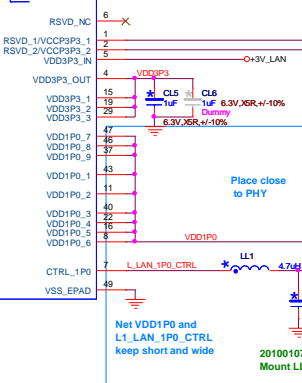
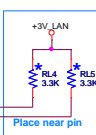
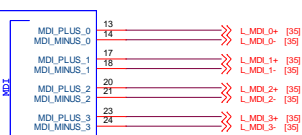
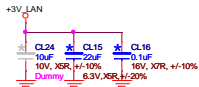


20091216 CRB0.7: Connect a series CL14 (10 pF) capacitor to XTAL_OUT (pin 9)

less than 325 mils



Close to PINS (VDD)

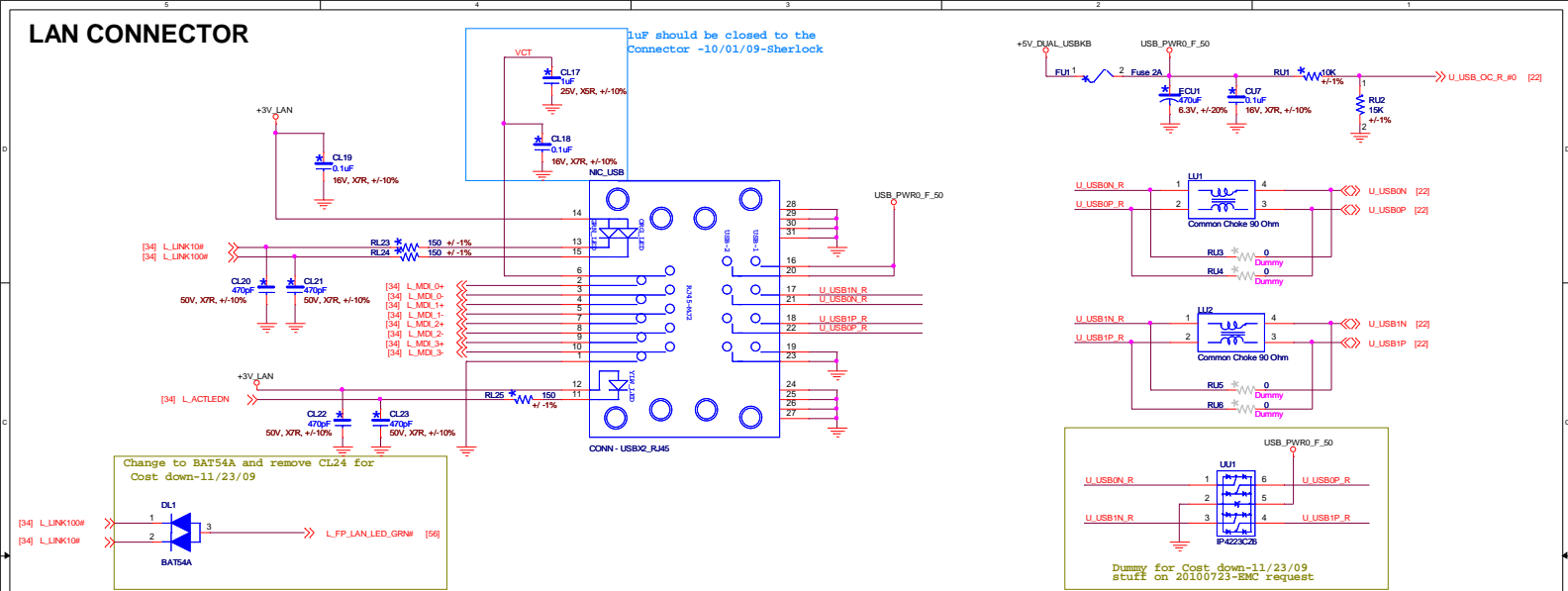


20091216 follow CRB0.7 and 82579 checklist: does not require any MDI termination.(delete => RL15, RL16, RL17, RL18, RL19, RL20, RL21, RL22, CL11, CL12, CL13, CL14)

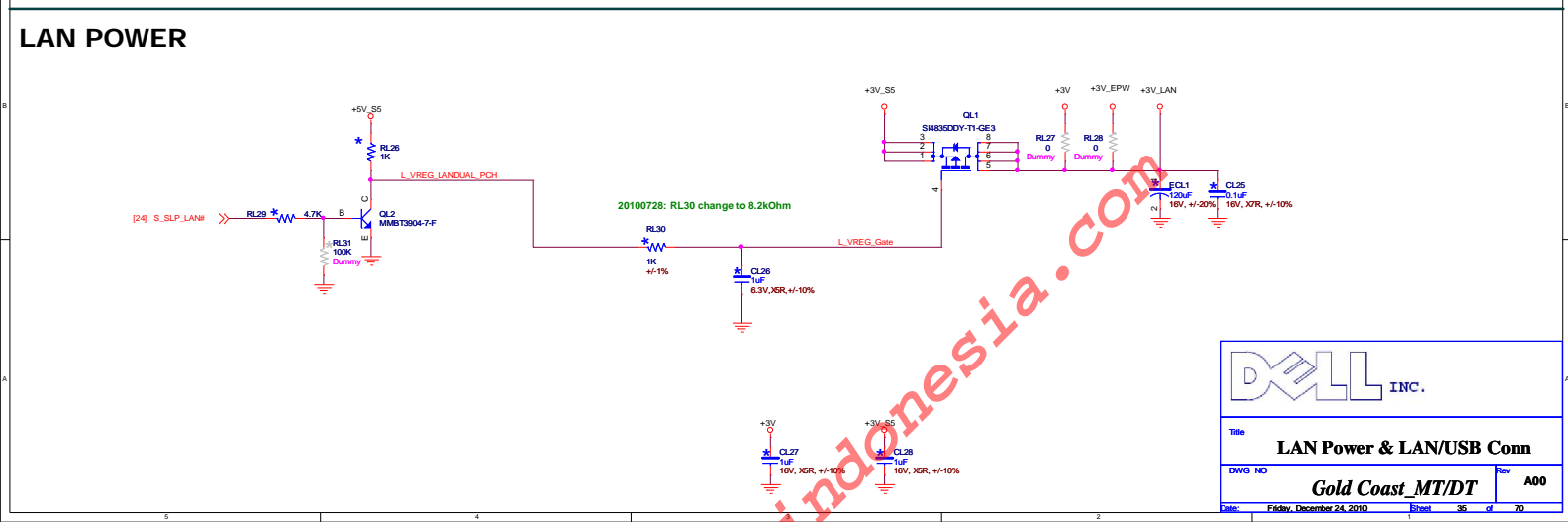


Title		
LAN: Intel Lewisvillies		
DWG NO	Rev	A00
Gold Coast_MT/DT		
Date	Friday, December 24, 2010	Sheet 34 of 70

LAN CONNECTOR



LAN POWER



DELL INC.		
Title	LAN Power & LAN/USB Conn	
DWG NO	Gold Coast_MT/DT	Rev A00
Date	Friday, December 24, 2010	Sheet 36 of 70

D

33

2

C

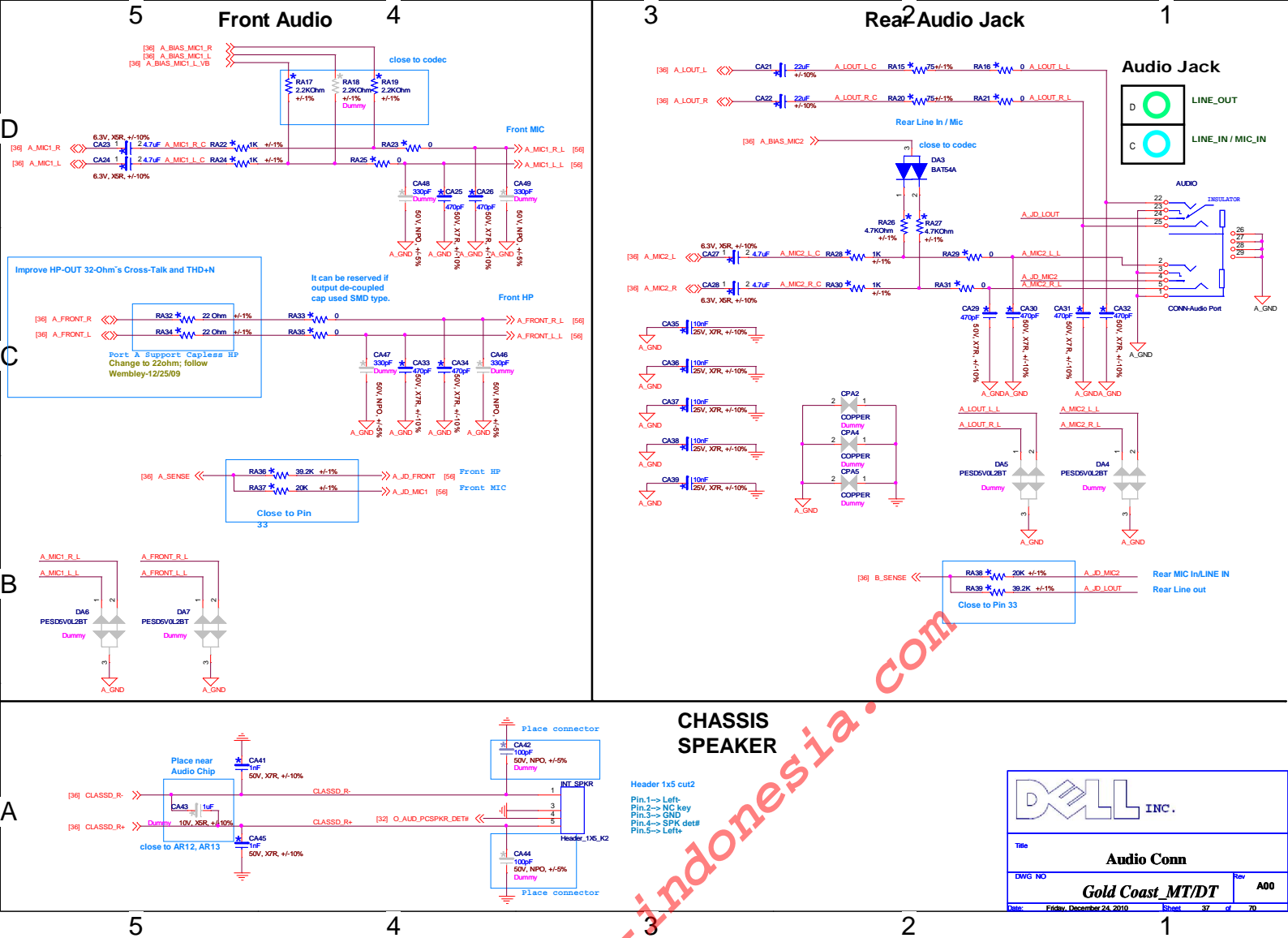
B

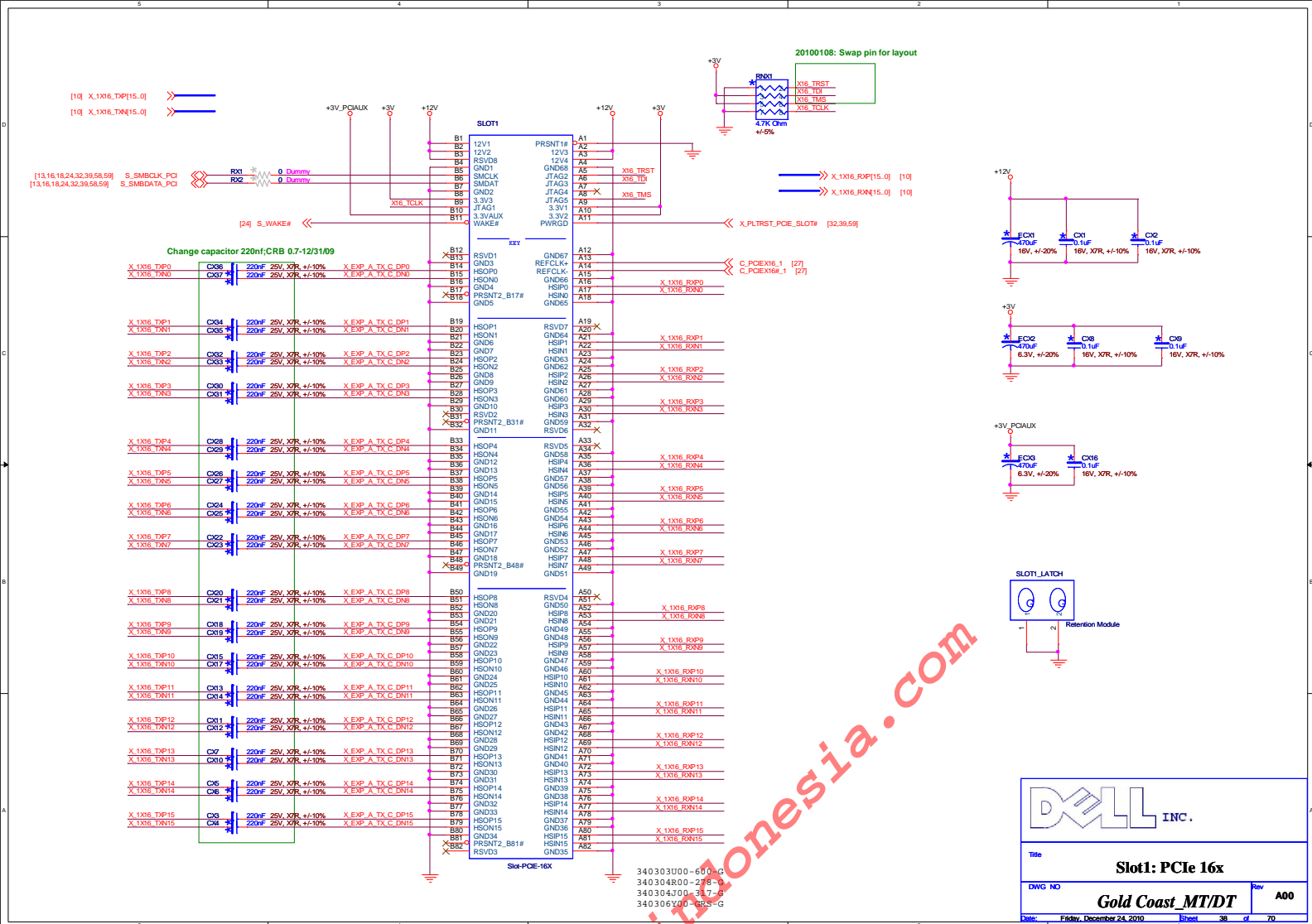
A

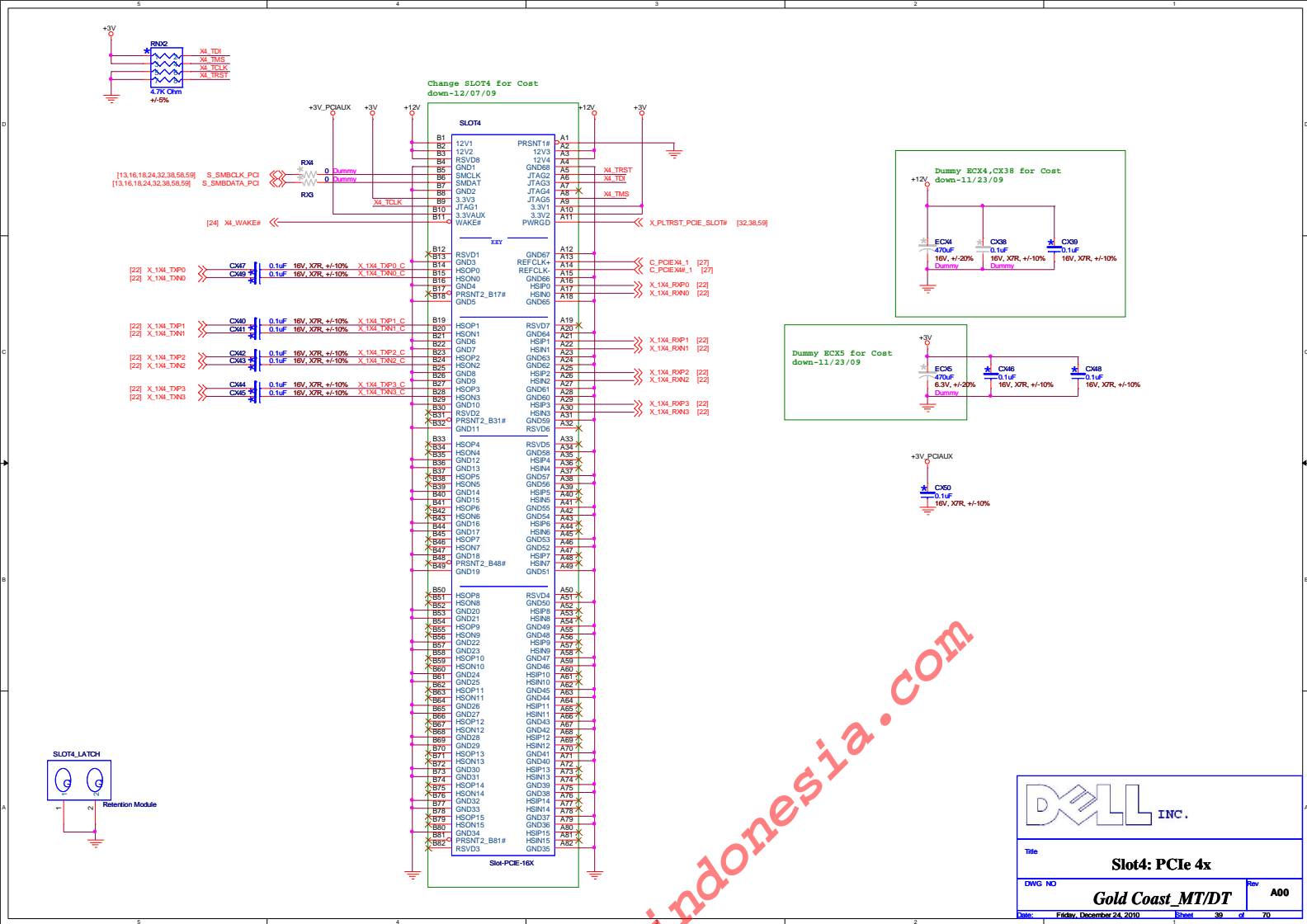
3

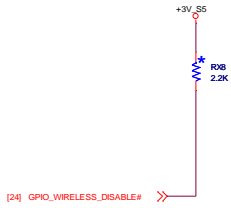
1

				INC.	
Title					
Audio ALC269Q					
DWG NO				Rev	
Gold Coast MT/DT				A00	
Date:	Friday, December 24, 2010	Sheet	36	of	70



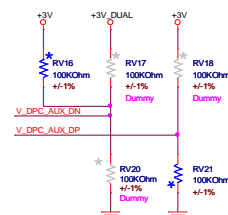
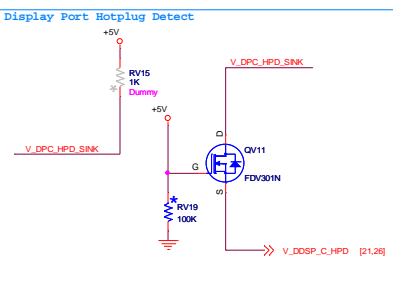
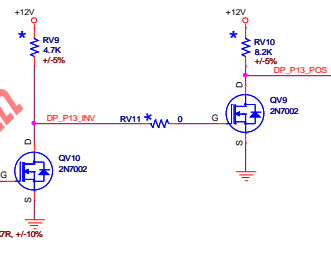
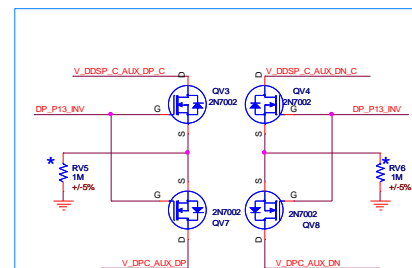
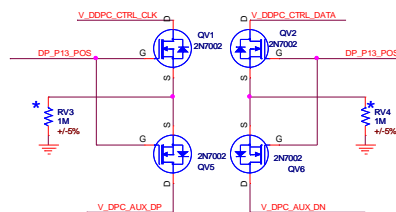
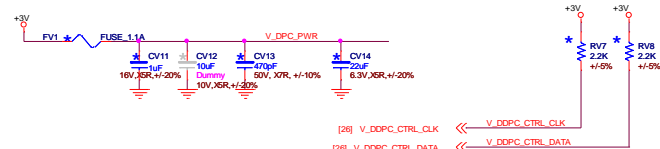
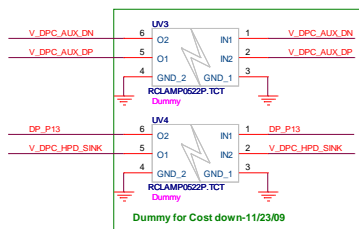
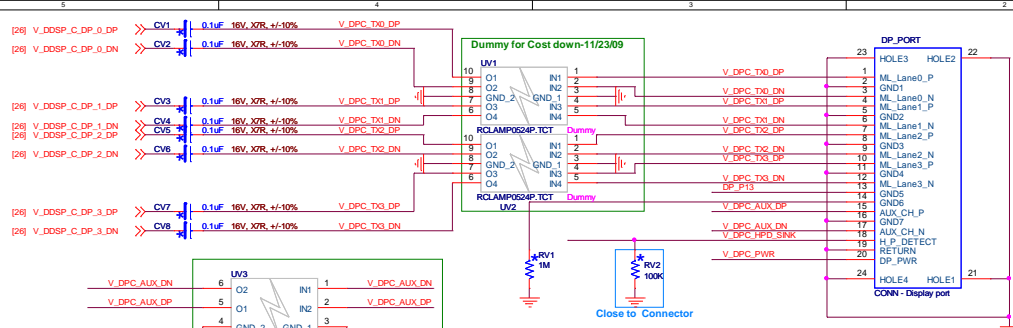






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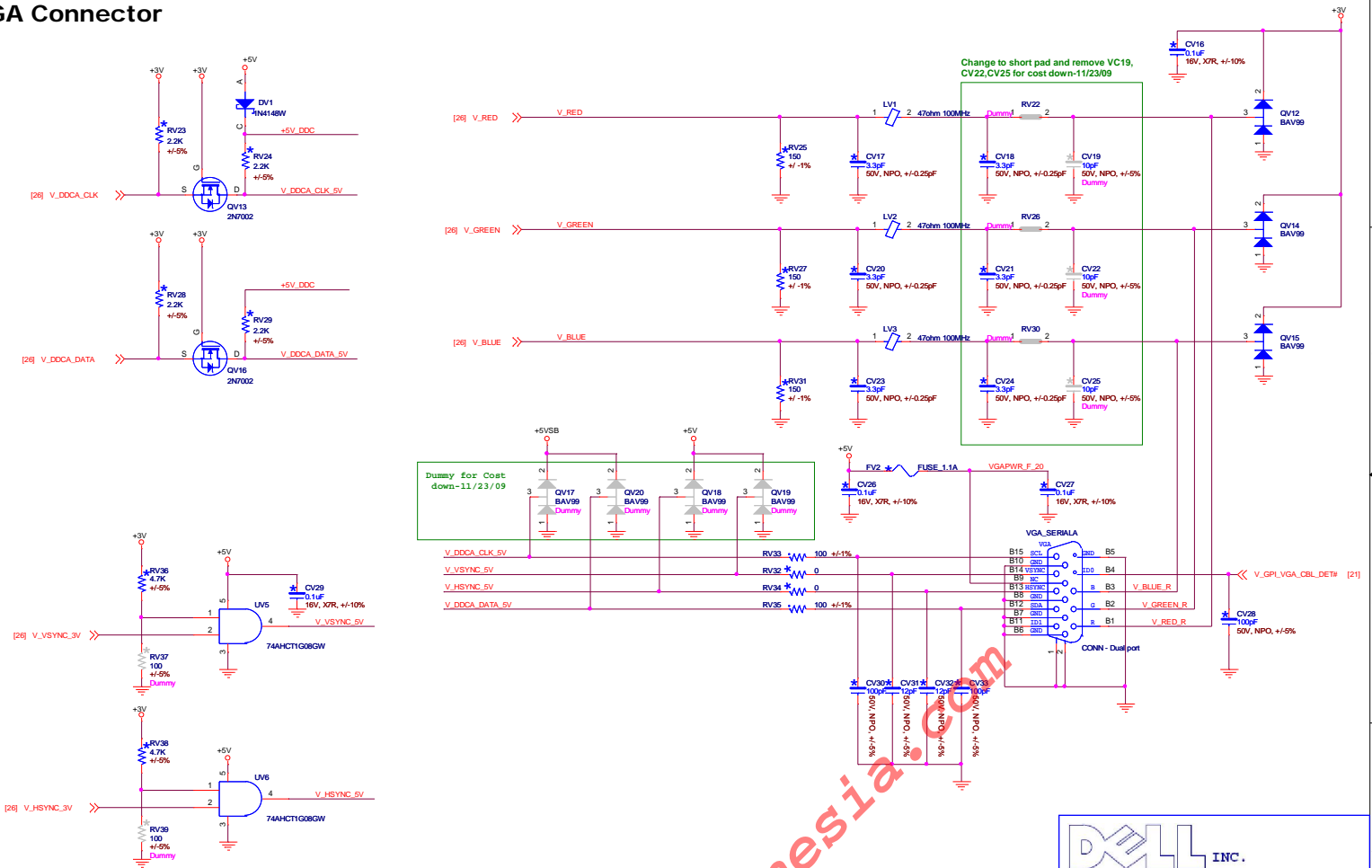
DELL INC.		
Title		
TBD		
DWG NO	Gold Coast_MT/DT	Rev A00
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INC.		
Title		
Display Port		
DWG NO	Gold Coast_MT/DT	Rev A00
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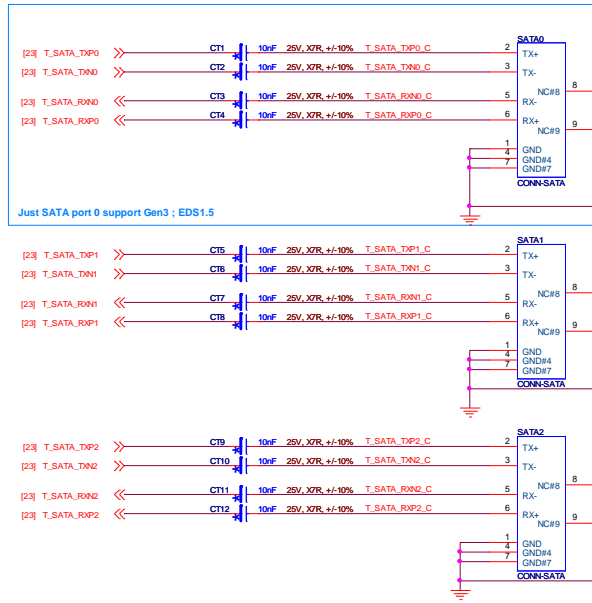
VGA Connector



**INC.**

Title		VGA Conn	
DWG NO	Gold Coast_MT/DT		Rev
		A00	
Date:	Friday, December 24, 2010	Sheet	42 of 70

SATA x 3

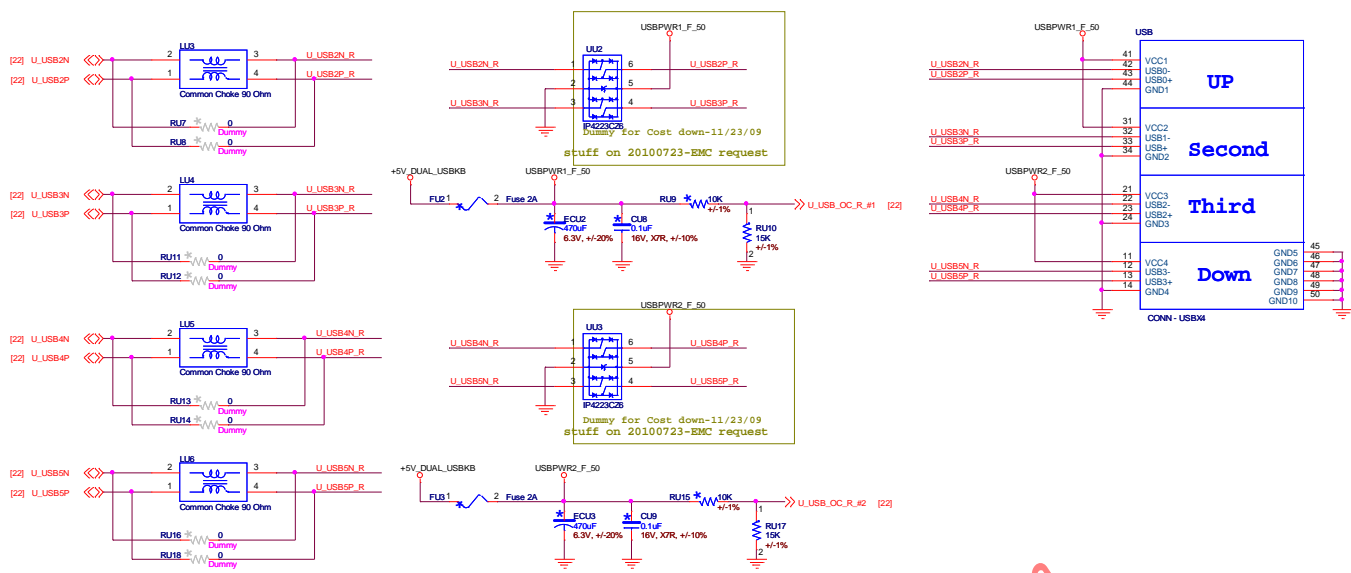


DELL INC.	
Title	
SATA Conn	
DWG NO	Rev
Gold Coast_MT/DT	A00
Date: Friday, December 24, 2010	Sheet 48 of 70

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Title TBD	
DWG NO	Rev A00
Gold Coast_MT/DT	
Date: Friday, December 24, 2010	Sheet 44 of 70

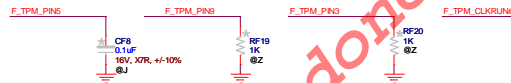
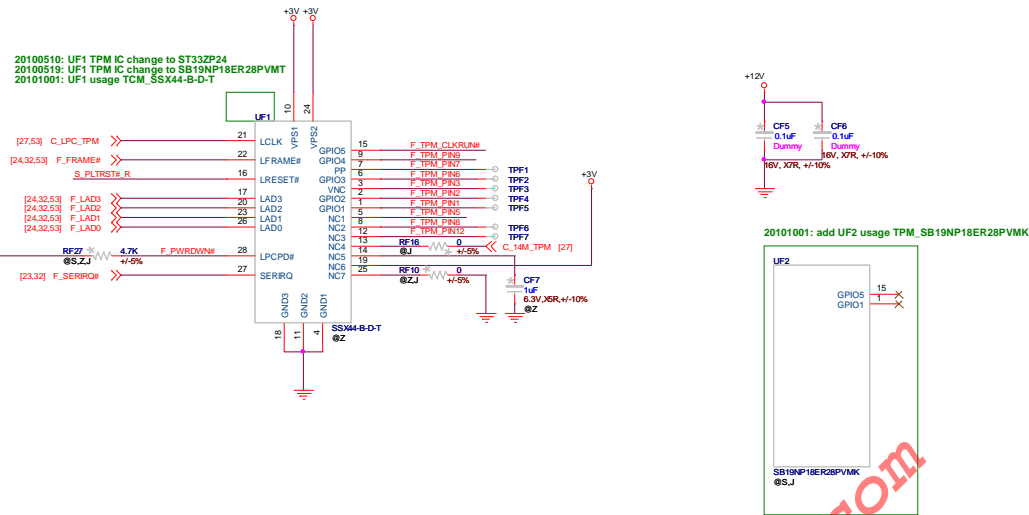
Rear USB CONNECTOR



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DELL INC.		
Title		
Rear USB		
DWG NO	Gold Coast_MT/DT	Rev A00
Date	Friday, December 24, 2010	Sheet 46 of 70

(Default) ST Micro	POP S	CF4
ZTE	POP Z	CF2,CF4,CF7,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21



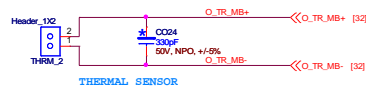
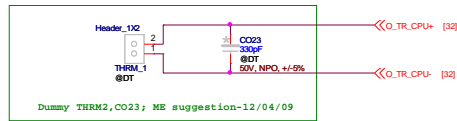
D

C

B

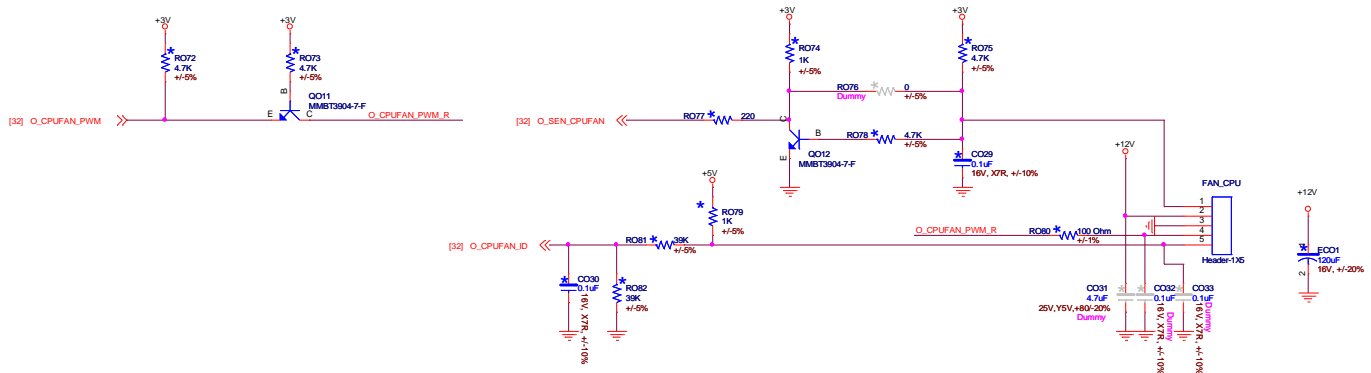
A

Change net to O_TR_MB+/-; SMSC suggestion-12/08/09
Removed THRM1 since useless-01/01/10

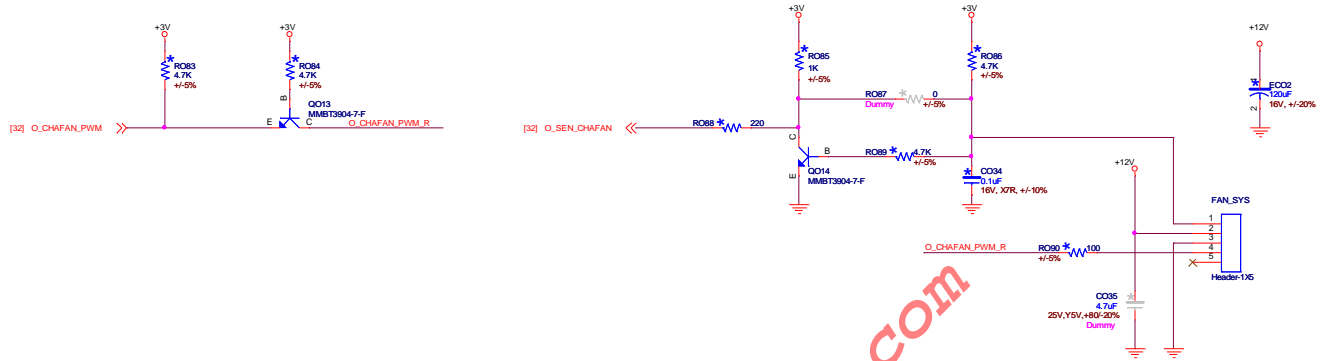


DELL INC.		
Title Thermal Sensor Conn		
DWG NO	Gold Coast MT/DT	Rev A00
Date: Friday, December 24, 2010 Sheet 47 of 70		

CPU Fan



SYS Fan

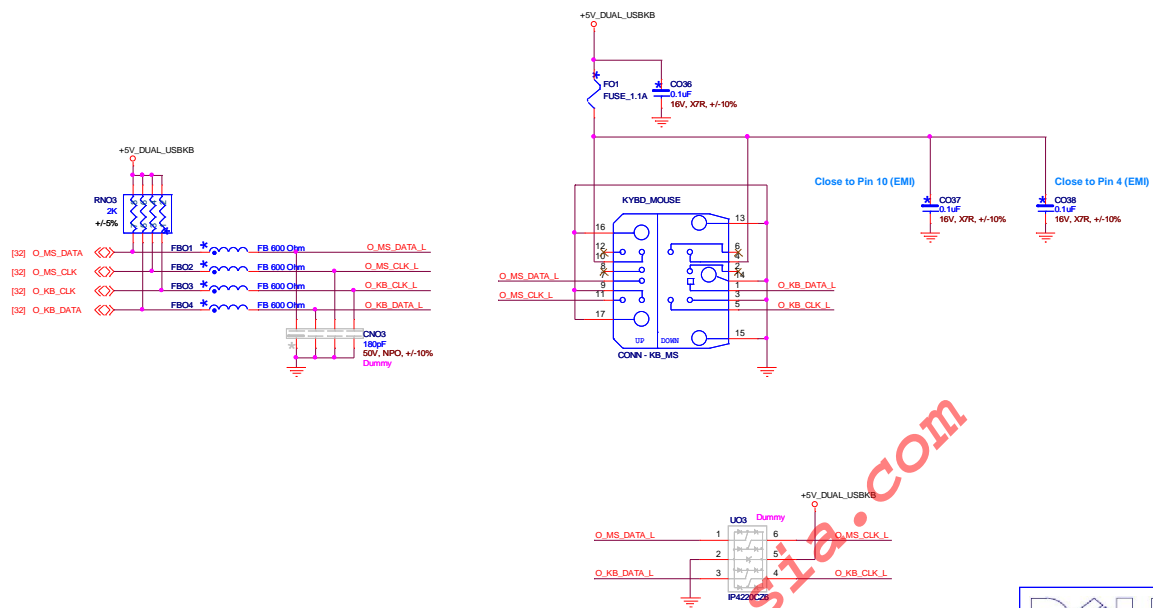


PSU Fan

20100111: Remove PSU PWM control

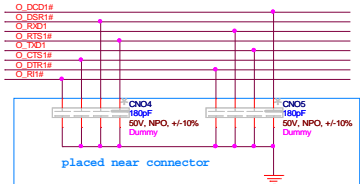
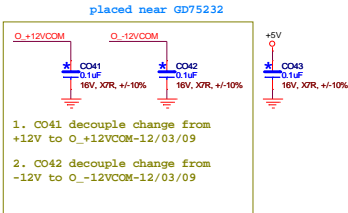
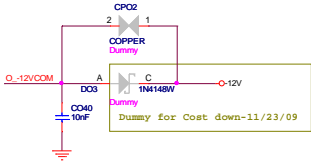
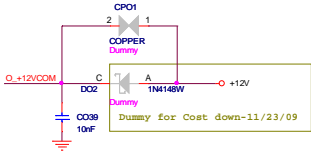
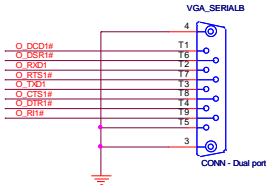
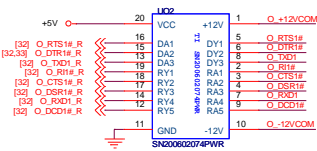


DELL INC.		
Title		
FAN		
DWG NO		Rev
Gold Coast_MT/DT		A00
Date: Friday, December 24, 2010		
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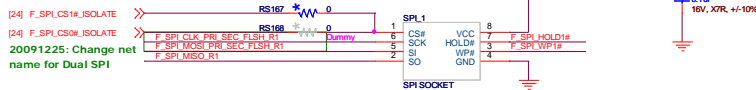
DELL INC.		
Title		
PS2 Conn		
DWG NO	Gold Coast_MT/DT	Rev A00
Date	Friday, December 24, 2010	Sheet 49 of 70

Serial Port 1



DELL INC.		
Title		
COM1		
DWG NO		Rev
Gold Coast_MT/DT		A00
Date: Friday, December 24, 2010 Sheet 50 of 70		

SPI



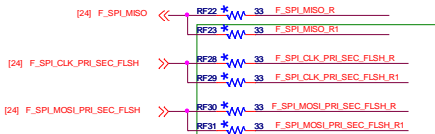
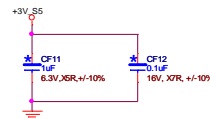
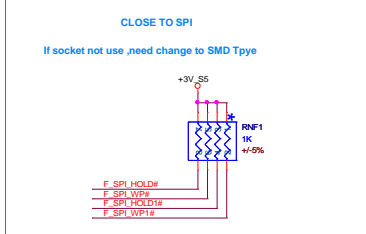
Dummy for cost down-11/23/09

20100329: SPI_ROM1 Package Type change to DIP from SMD, when usage SPI1 socket

20100512: SPI_ROM1 change to NUMONVX_M25PX16-VMMW6TG and mount

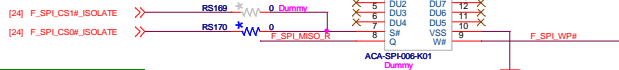
20100512: SPI_ROM1 rename to SPI1

20100930: SPI1 change to MXIC_MX25L1606EM2I-12G



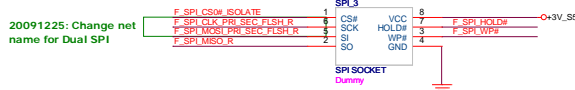
20091225: RF23 change to 33ohm for Dual SPI

20091225: Add RF28, RF29, RF30, RF31 for Dual SPI



20100309: SPI2 Package Type change to DIP from SMD, when usage SPI2 socket

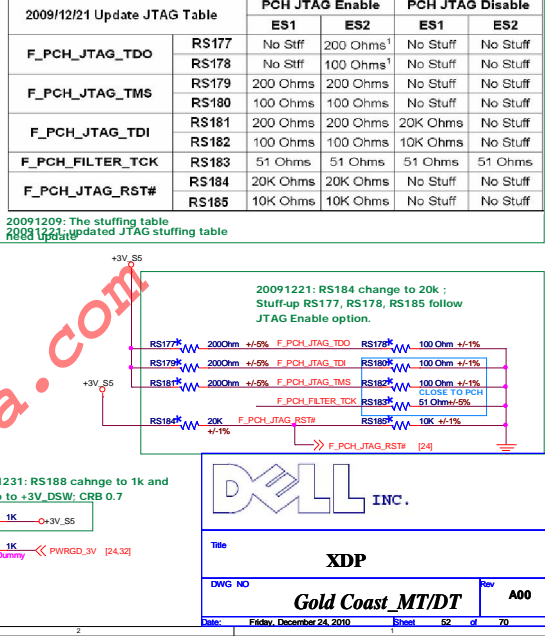
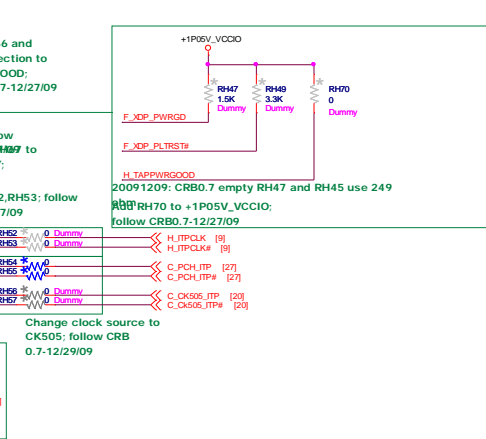
20100930: SPI2 change to MXIC_MX25L6445EM1-10G



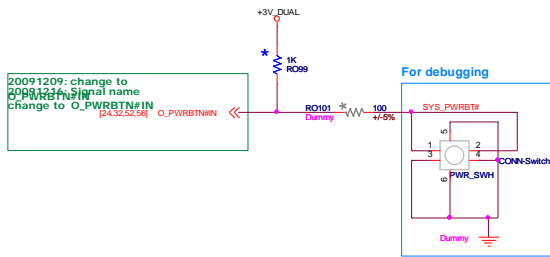
SPI	
DWG NO	Rev
Gold Coast_MT/DT	A00
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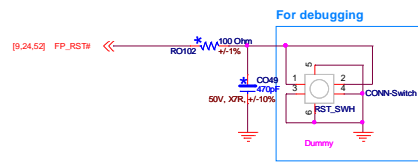
XDP Connector - PCH



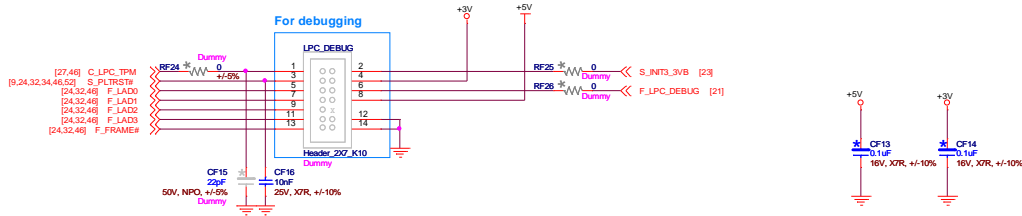
Power Bottom



Reset Bottom

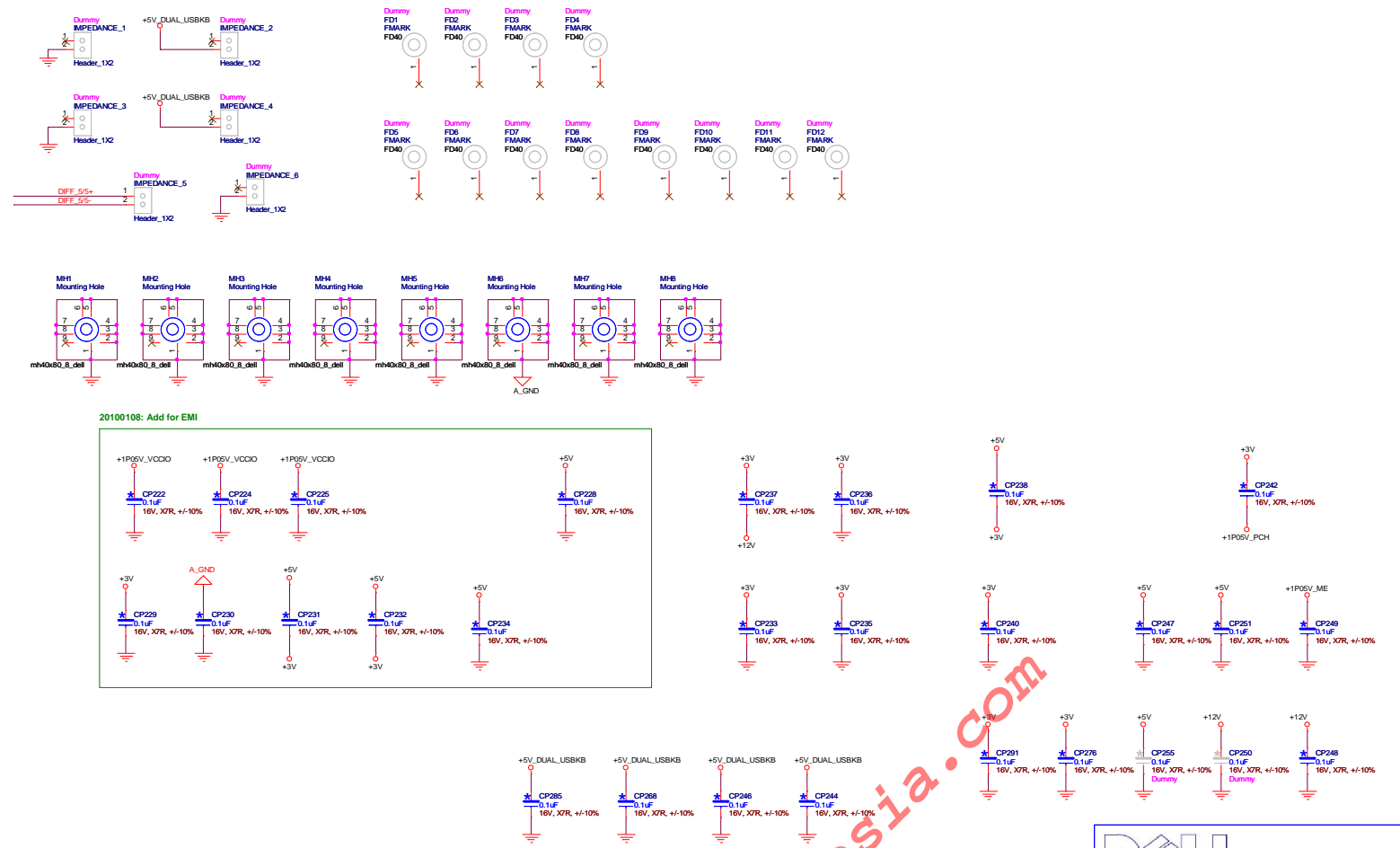


LPC DEBUG



DELL INC.		
Title		
Pilot Run Conn		
DWG NO	Gold Coast_MT/DT	Rev A00
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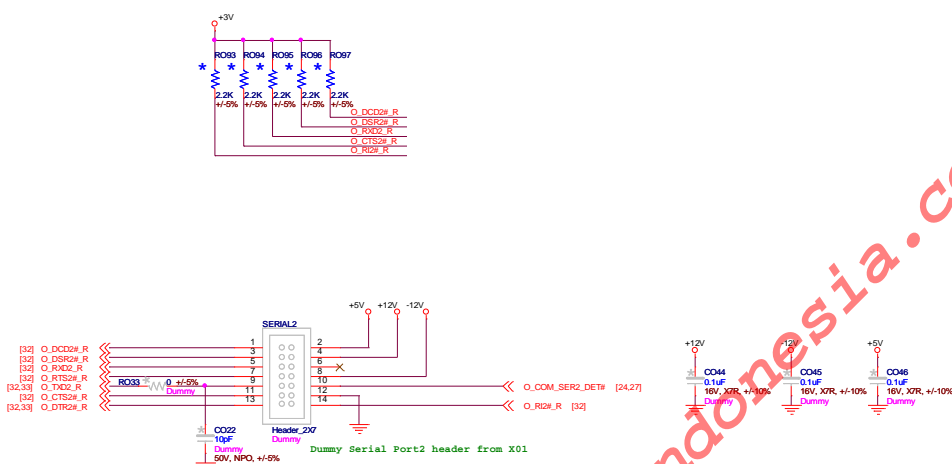
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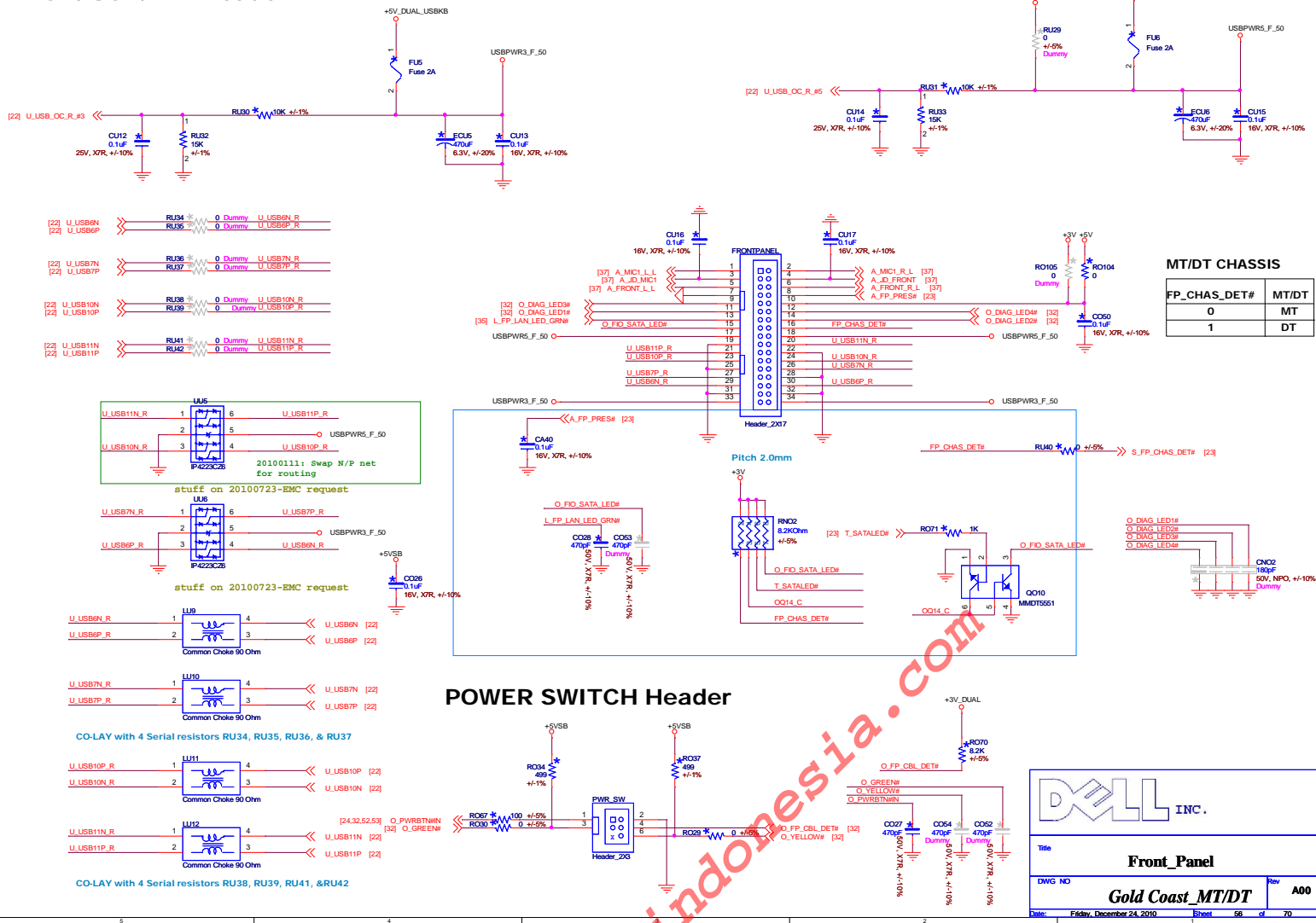
Title		
EMI		
DWG NO	Gold Coast_MT/DT	Rev A00
Date	Friday, December 24, 2010	Sheet 54 of 70

Move PWR_SW conn to
page56 20091126

Serial Port 2 Header



Front USB/LED Header



POWER SWITCH Header

The schematic diagram illustrates the electrical connections for the POWER SWITCH Header. The header is a 5-pin connector labeled 'PWR_SW Header_0X3'. The connections are as follows:

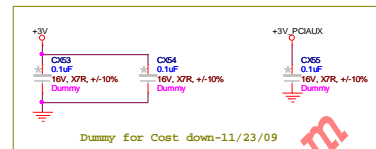
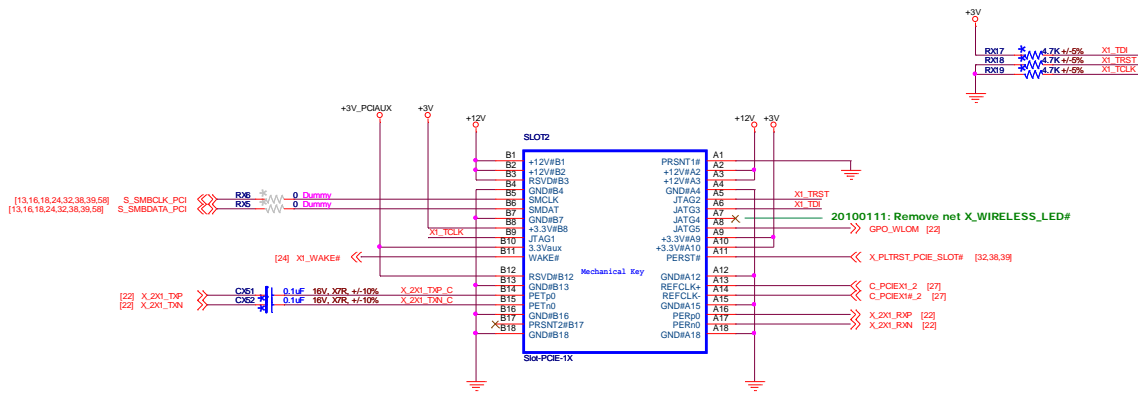
- Pin 1:** Connected to +5VSB through resistor RO34 (400, +/-1%).
- Pin 2:** Connected to +5VSB through resistor RO37 (499, +/-1%).
- Pin 3:** Connected to a network of resistors: RO67 (400, +/-5%), RO30 (0, +/-5%), and RO36 (100, +/-5%).
- Pin 4:** Connected to a network of resistors: RO28 (0, +/-5%), RO38 (0, +/-5%), and RO39 (0, +/-5%).
- Pin 5:** Connected to ground.

Additional components and connections shown in the diagram include:

- Capacitors CO27 (470pF), CO54 (470pF), and CO55 (470pF) connected to ground.
- Resistors RO1 (8.2k, +/-5%), RO2 (10k, +/-5%), and RO3 (10k, +/-5%) connected to +3V_DUAL.
- Resistor RO4 (10k, +/-5%) connected to +5VSB.
- Resistor RO5 (10k, +/-5%) connected to +5VSB.
- Resistor RO6 (10k, +/-5%) connected to +5VSB.
- Resistor RO7 (10k, +/-5%) connected to +5VSB.
- Resistor RO8 (10k, +/-5%) connected to +5VSB.
- Resistor RO9 (10k, +/-5%) connected to +5VSB.
- Resistor RO10 (10k, +/-5%) connected to +5VSB.
- Resistor RO11 (10k, +/-5%) connected to +5VSB.
- Resistor RO12 (10k, +/-5%) connected to +5VSB.
- Resistor RO13 (10k, +/-5%) connected to +5VSB.
- Resistor RO14 (10k, +/-5%) connected to +5VSB.
- Resistor RO15 (10k, +/-5%) connected to +5VSB.
- Resistor RO16 (10k, +/-5%) connected to +5VSB.
- Resistor RO17 (10k, +/-5%) connected to +5VSB.
- Resistor RO18 (10k, +/-5%) connected to +5VSB.
- Resistor RO19 (10k, +/-5%) connected to +5VSB.
- Resistor RO20 (10k, +/-5%) connected to +5VSB.
- Resistor RO21 (10k, +/-5%) connected to +5VSB.
- Resistor RO22 (10k, +/-5%) connected to +5VSB.
- Resistor RO23 (10k, +/-5%) connected to +5VSB.
- Resistor RO24 (10k, +/-5%) connected to +5VSB.
- Resistor RO25 (10k, +/-5%) connected to +5VSB.
- Resistor RO26 (10k, +/-5%) connected to +5VSB.
- Resistor RO27 (10k, +/-5%) connected to +5VSB.
- Resistor RO28 (10k, +/-5%) connected to +5VSB.
- Resistor RO29 (10k, +/-5%) connected to +5VSB.
- Resistor RO30 (10k, +/-5%) connected to +5VSB.
- Resistor RO31 (10k, +/-5%) connected to +5VSB.
- Resistor RO32 (10k, +/-5%) connected to +5VSB.
- Resistor RO33 (10k, +/-5%) connected to +5VSB.
- Resistor RO34 (10k, +/-5%) connected to +5VSB.
- Resistor RO35 (10k, +/-5%) connected to +5VSB.
- Resistor RO36 (10k, +/-5%) connected to +5VSB.
- Resistor RO37 (10k, +/-5%) connected to +5VSB.
- Resistor RO38 (10k, +/-5%) connected to +5VSB.
- Resistor RO39 (10k, +/-5%) connected to +5VSB.
- Resistor RO40 (10k, +/-5%) connected to +5VSB.
- Resistor RO41 (10k, +/-5%) connected to +5VSB.
- Resistor RO42 (10k, +/-5%) connected to +5VSB.
- Resistor RO43 (10k, +/-5%) connected to +5VSB.
- Resistor RO44 (10k, +/-5%) connected to +5VSB.
- Resistor RO45 (10k, +/-5%) connected to +5VSB.
- Resistor RO46 (10k, +/-5%) connected to +5VSB.
- Resistor RO47 (10k, +/-5%) connected to +5VSB.
- Resistor RO48 (10k, +/-5%) connected to +5VSB.
- Resistor RO49 (10k, +/-5%) connected to +5VSB.
- Resistor RO50 (10k, +/-5%) connected to +5VSB.
- Resistor RO51 (10k, +/-5%) connected to +5VSB.
- Resistor RO52 (10k, +/-5%) connected to +5VSB.
- Resistor RO53 (10k, +/-5%) connected to +5VSB.
- Resistor RO54 (10k, +/-5%) connected to +5VSB.
- Resistor RO55 (10k, +/-5%) connected to +5VSB.
- Resistor RO56 (10k, +/-5%) connected to +5VSB.
- Resistor RO57 (10k, +/-5%) connected to +5VSB.
- Resistor RO58 (10k, +/-5%) connected to +5VSB.
- Resistor RO59 (10k, +/-5%) connected to +5VSB.
- Resistor RO60 (10k, +/-5%) connected to +5VSB.
- Resistor RO61 (10k, +/-5%) connected to +5VSB.
- Resistor RO62 (10k, +/-5%) connected to +5VSB.
- Resistor RO63 (10k, +/-5%) connected to +5VSB.
- Resistor RO64 (10k, +/-5%) connected to +5VSB.
- Resistor RO65 (10k, +/-5%) connected to +5VSB.
- Resistor RO66 (10k, +/-5%) connected to +5VSB.
- Resistor RO67 (10k, +/-5%) connected to +5VSB.
- Resistor RO68 (10k, +/-5%) connected to +5VSB.
- Resistor RO69 (10k, +/-5%) connected to +5VSB.
- Resistor RO70 (10k, +/-5%) connected to +5VSB.
- Resistor RO71 (10k, +/-5%) connected to +5VSB.
- Resistor RO72 (10k, +/-5%) connected to +5VSB.
- Resistor RO73 (10k, +/-5%) connected to +5VSB.
- Resistor RO74 (10k, +/-5%) connected to +5VSB.
- Resistor RO75 (10k, +/-5%) connected to +5VSB.
- Resistor RO76 (10k, +/-5%) connected to +5VSB.
- Resistor RO77 (10k, +/-5%) connected to +5VSB.
- Resistor RO78 (10k, +/-5%) connected to +5VSB.
- Resistor RO79 (10k, +/-5%) connected to +5VSB.
- Resistor RO80 (10k, +/-5%) connected to +5VSB.
- Resistor RO81 (10k, +/-5%) connected to +5VSB.
- Resistor RO82 (10k, +/-5%) connected to +5VSB.
- Resistor RO83 (10k, +/-5%) connected to +5VSB.
- Resistor RO84 (10k, +/-5%) connected to +5VSB.
- Resistor RO85 (10k, +/-5%) connected to +5VSB.
- Resistor RO86 (10k, +/-5%) connected to +5VSB.
- Resistor RO87 (10k, +/-5%) connected to +5VSB.
- Resistor RO88 (10k, +/-5%) connected to +5VSB.
- Resistor RO89 (10k, +/-5%) connected to +5VSB.
- Resistor RO90 (10k, +/-5%) connected to +5VSB.
- Resistor RO91 (10k, +/-5%) connected to +5VSB.
- Resistor RO92 (10k, +/-5%) connected to +5VSB.
- Resistor RO93 (10k, +/-5%) connected to +5VSB.
- Resistor RO94 (10k, +/-5%) connected to +5VSB.
- Resistor RO95 (10k, +/-5%) connected to +5VSB.
- Resistor RO96 (10k, +/-5%) connected to +5VSB.
- Resistor RO97 (10k, +/-5%) connected to +5VSB.
- Resistor RO98 (10k, +/-5%) connected to +5VSB.
- Resistor RO99 (10k, +/-5%) connected to +5VSB.
- Resistor RO100 (10k, +/-5%) connected to +5VSB.

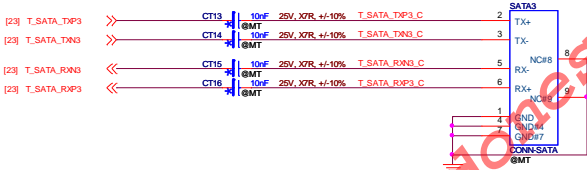
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 INC.	
Title TBD	
DWG NO	Rev A00
Gold Coast_MT/DT	
Date: Friday, December 24, 2010	Sheet 57 of 70

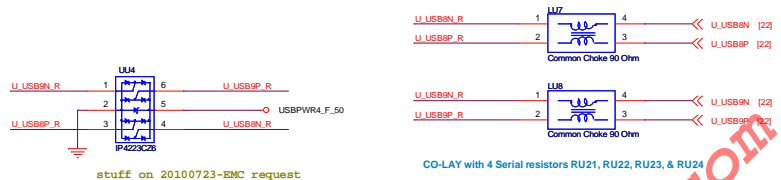


		
INC.		
Title		
Slot2: PCIe 1x		
DWG NO	Rev	A00
Gold Coast_MT/DT		
Date	Friday, December 24, 2010	Sheet 59 of 70

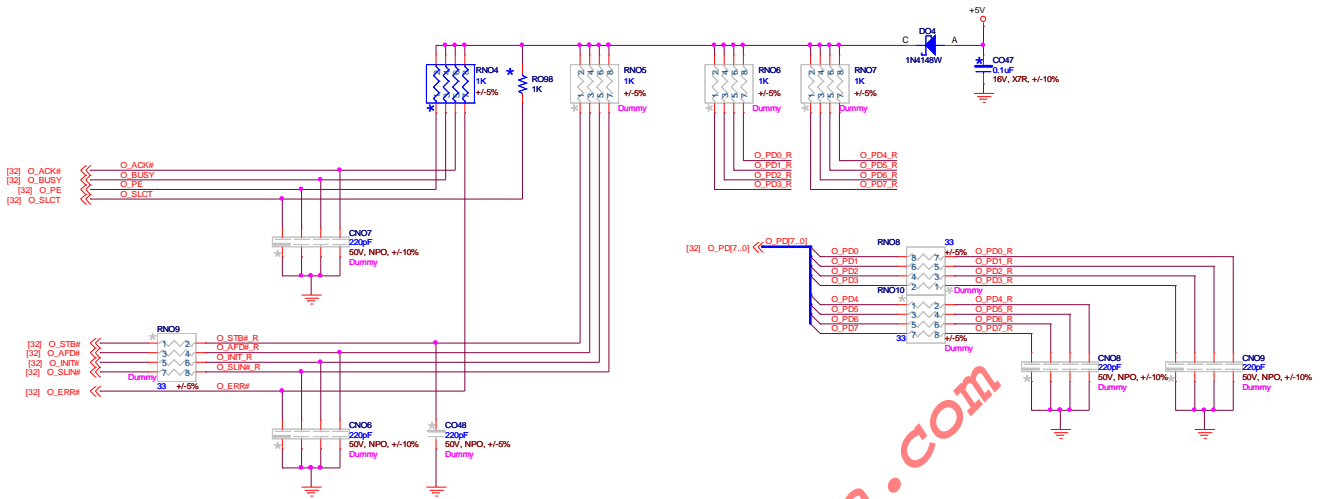
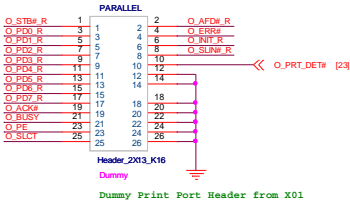
SATA port 3 only for MT



Title		
SATA_MT		
DWG NO	Rev	A00
Date: Friday, December 24, 2010 Sheet 60 of 70		

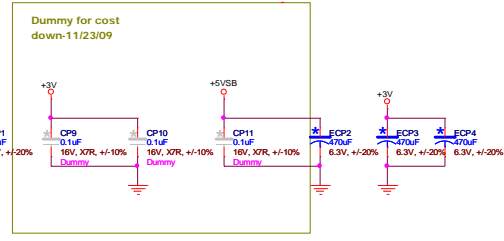
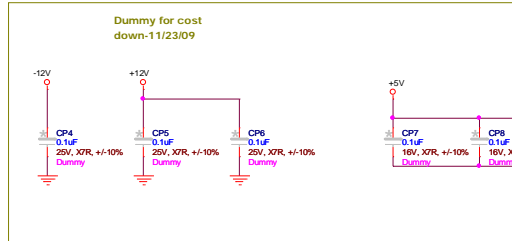
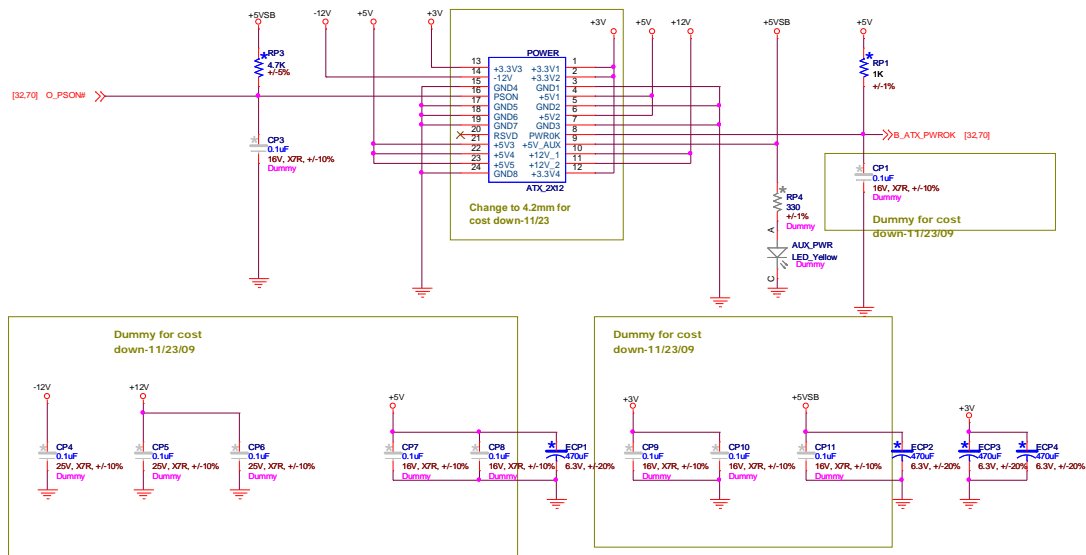


Print Port



DELL INC.	
Title	
PRT Port	
DWG NO	Rev
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ATX POWER CONNECTOR



Title	
Power Conn	
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+3V_EPW

[24,32,66] S_SLP_MH

+3V_S5

RP211 0 Dummy

+3V_EPW

RP224 10K

RP228 0

QPB8 PDS340P

CP27 4.7uF Dummy

CP42 0.1uF Dummy

CP156 4.7uF Dummy

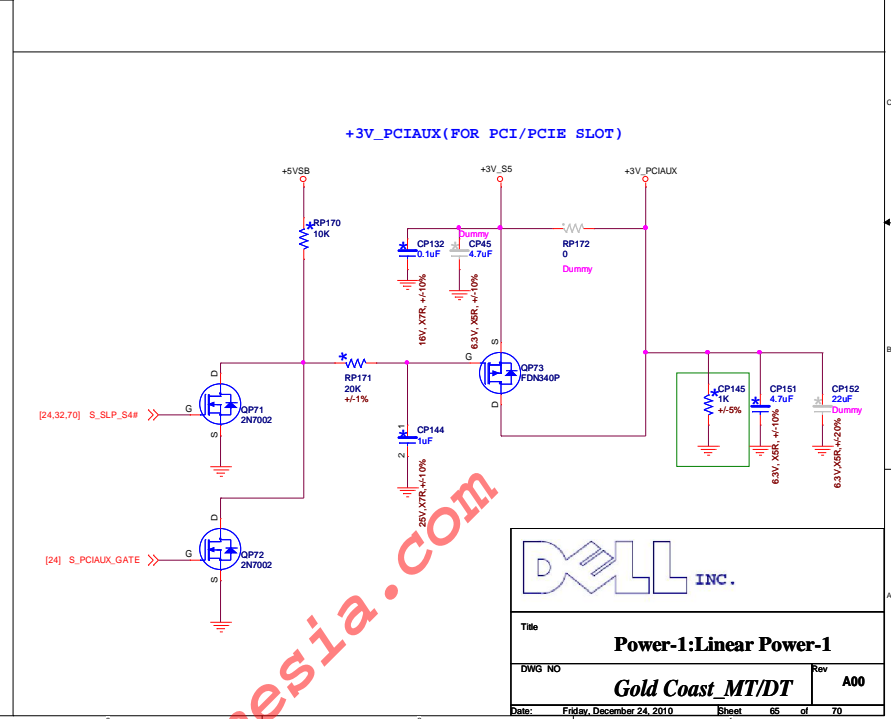
6.3V_XSR, +/-10%

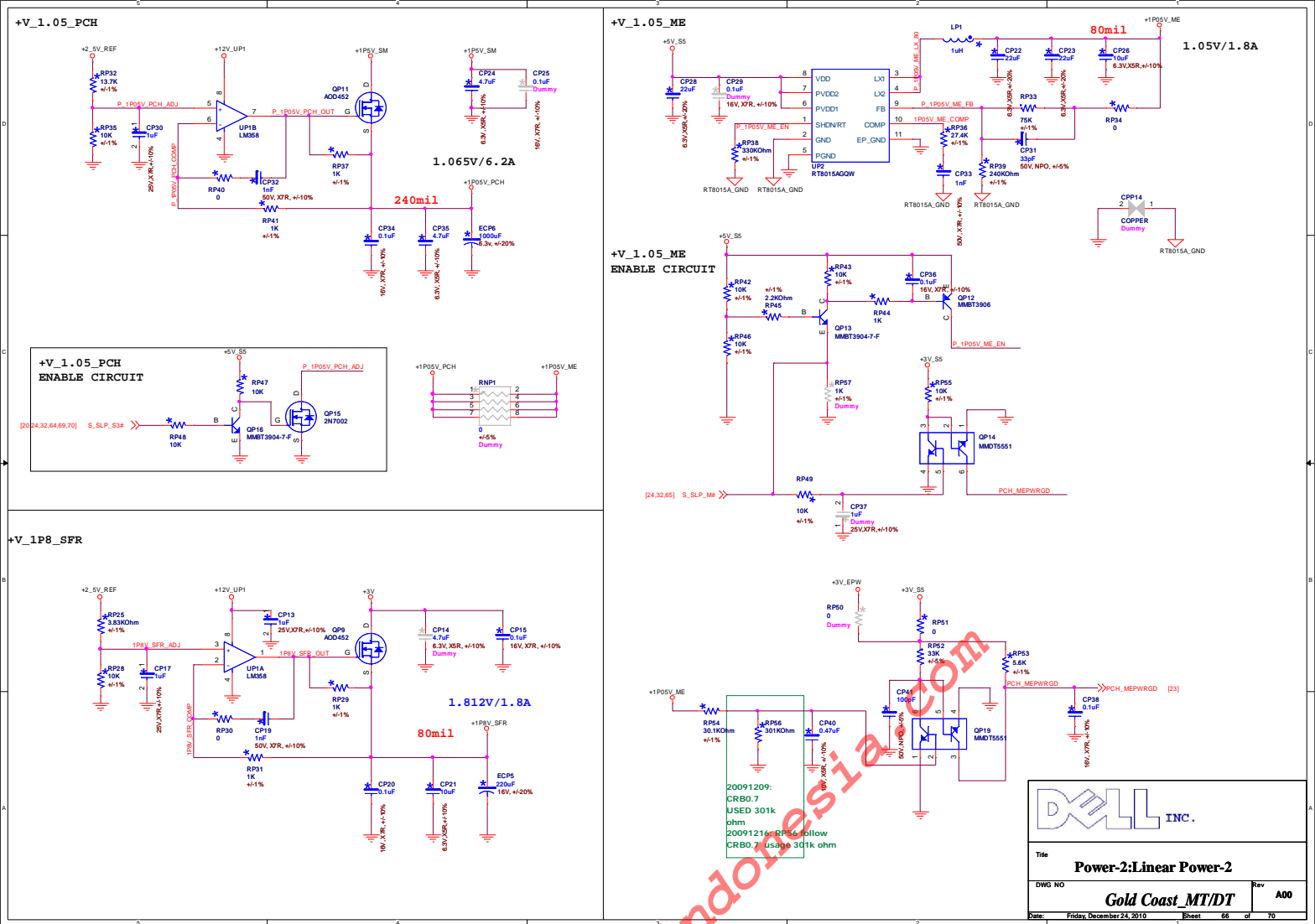
16V_XTR, +/-10%

25V_XTR, +/-10%

25V_XSR, +/-10%

20100709: Reserve RP210 connect +3V_S5 to +3V_EPW

[illegible]



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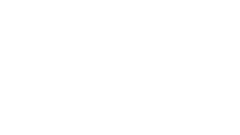
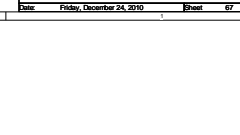
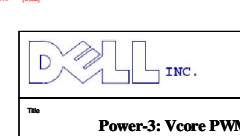
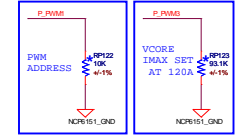
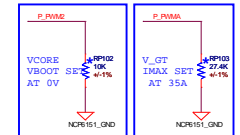
Sugar Bay VR12 POWER - 4+1 PHASE

VCC_CORE

VCC_AXG

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

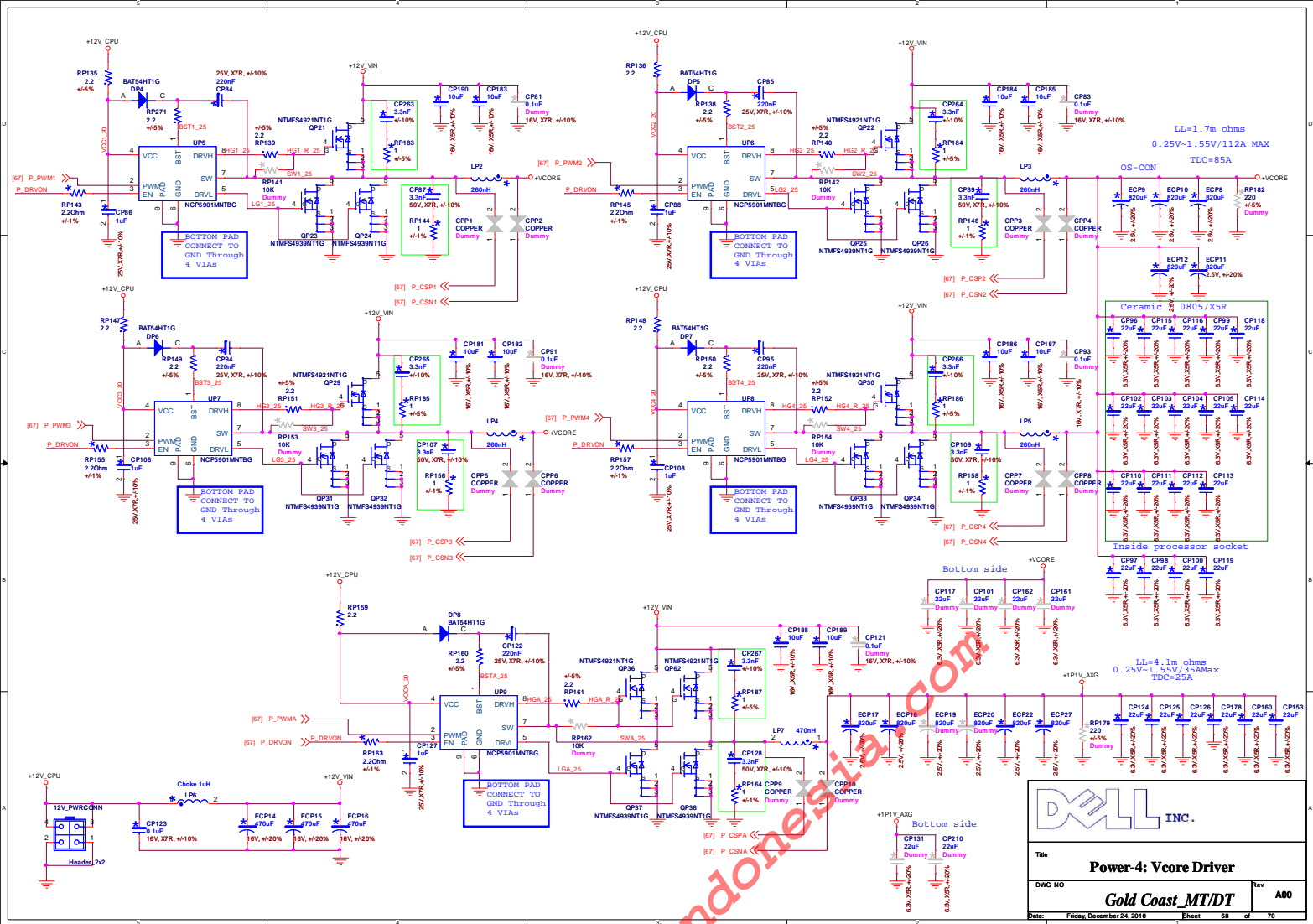
BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
125K	1.1V
165K	1.5V

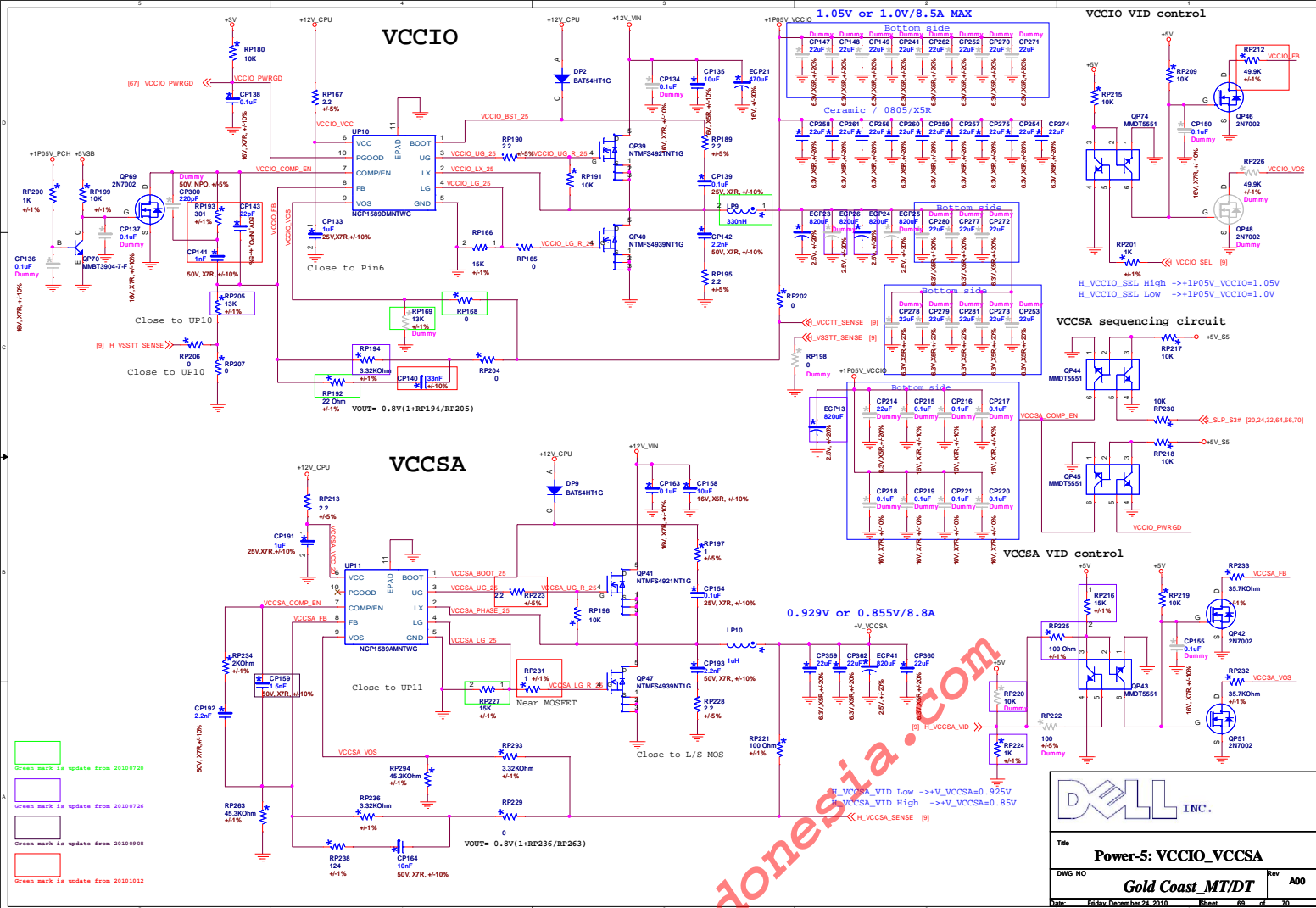


Power-3: Vcore PWM
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+V_1.5_SM Power(DDRIII)

