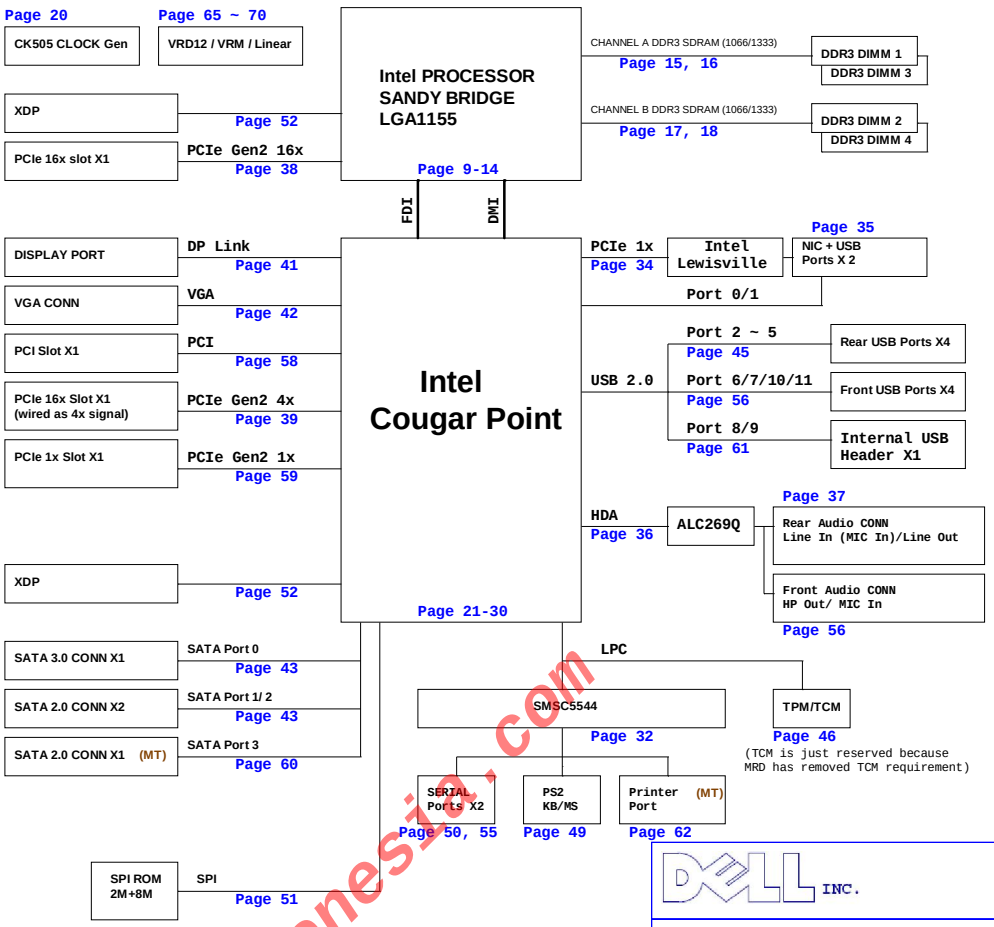
# Gold Coast- MT / DT








DELL INC.

Title: Index / Block diagram

DWG NO: Gold Coast_MT/DT

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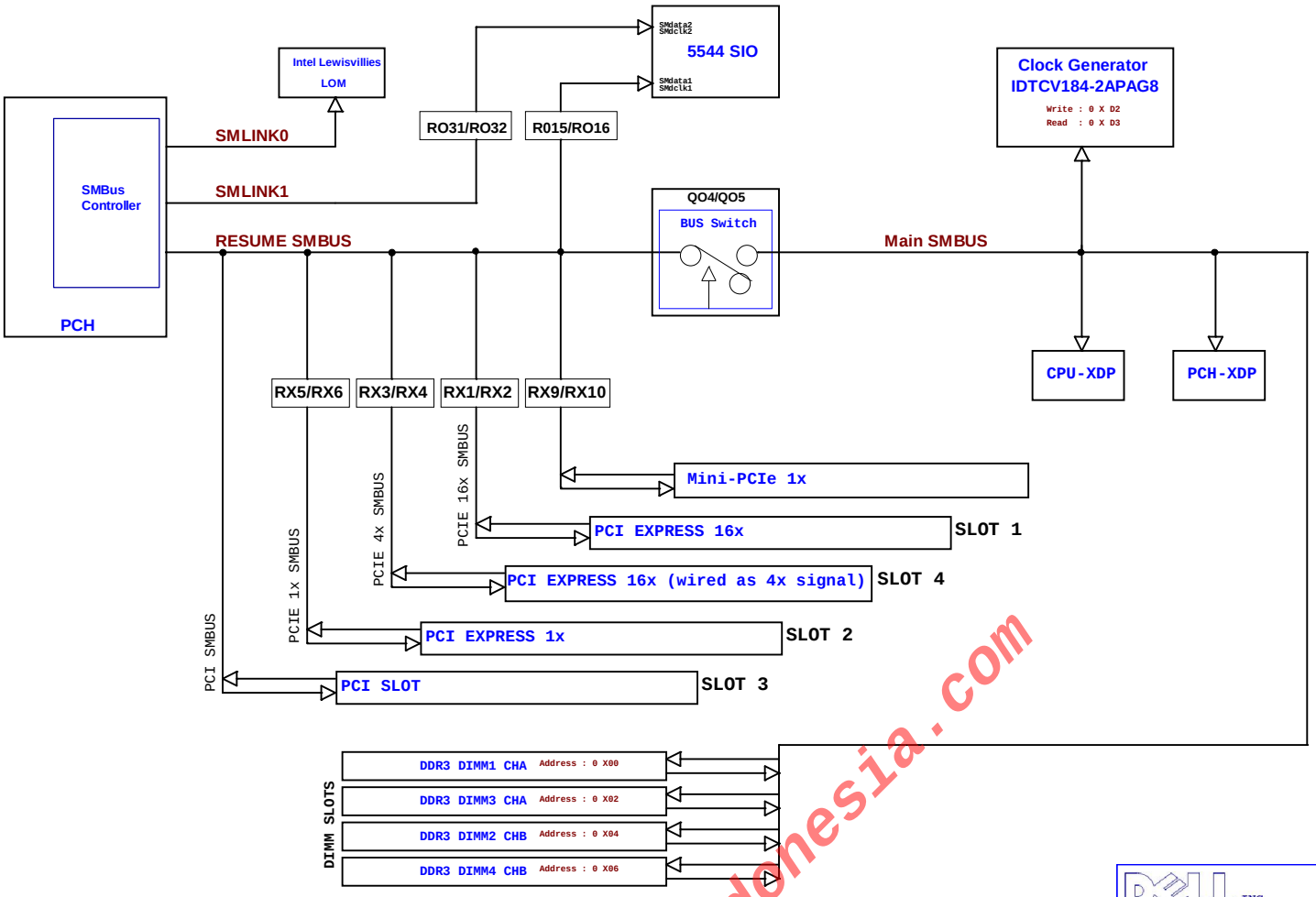
# SMBUS DIAGRAM




DELL INC.

Title: BLOCK DIAGRAM

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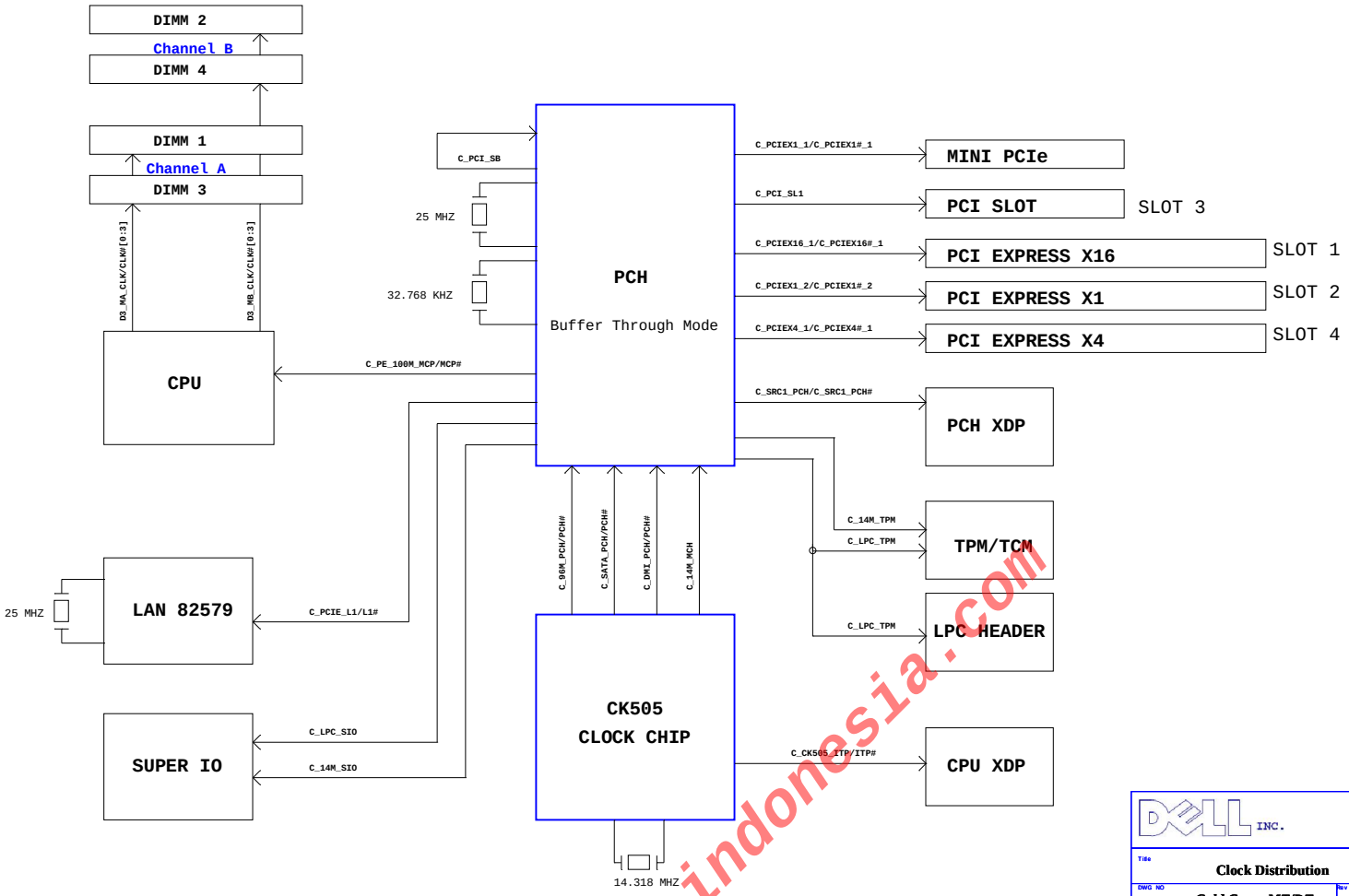
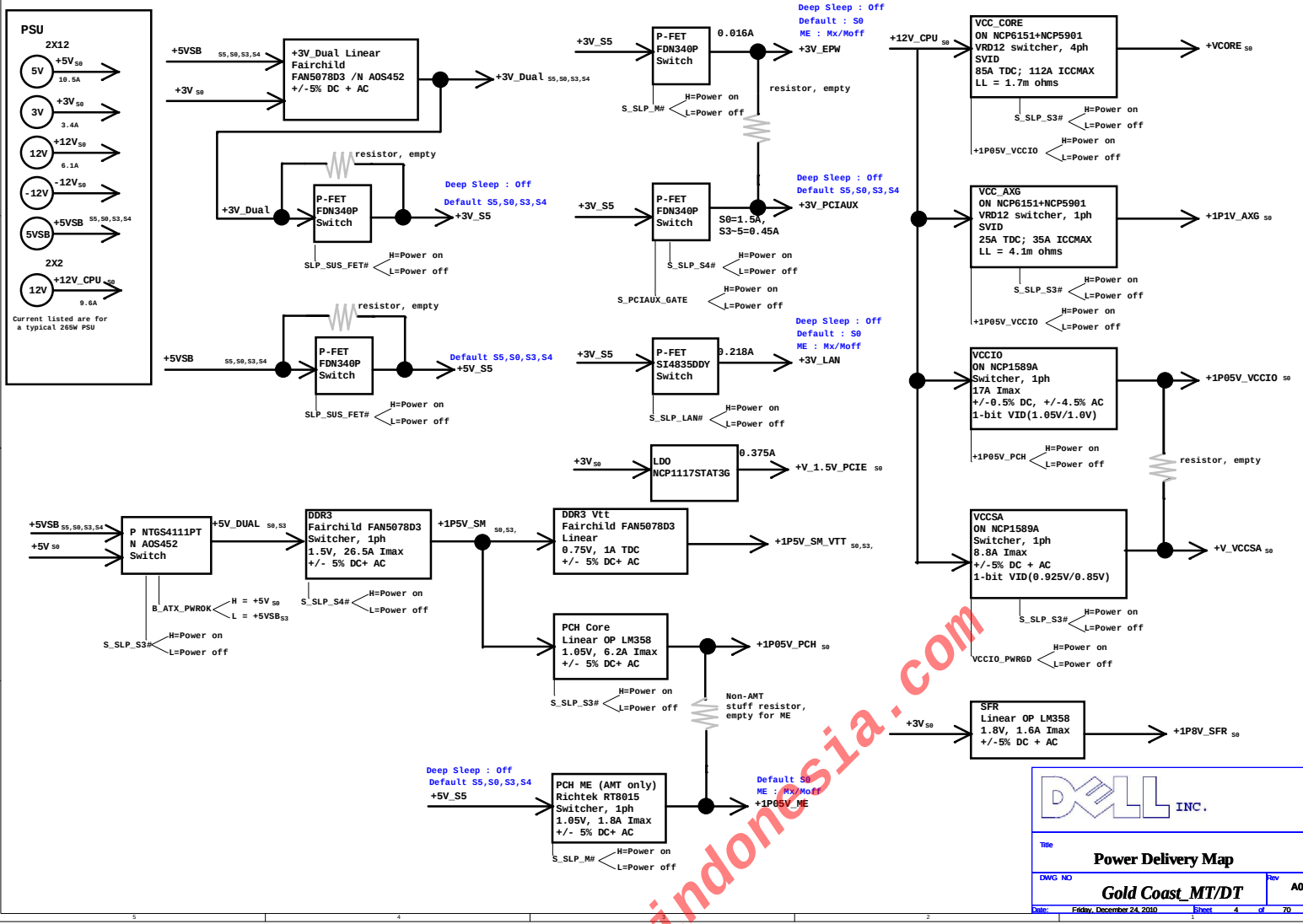


# POWER DELIVERY MAP




DELL INC.

Title: Power Delivery Map

DWG NO: Gold Coast_MT/DT

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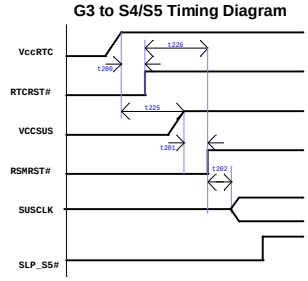
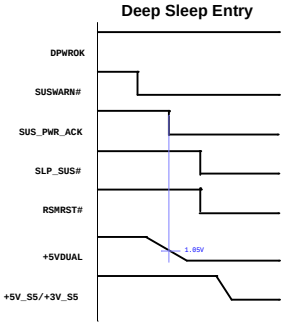
# POWER ON Timing Diagram

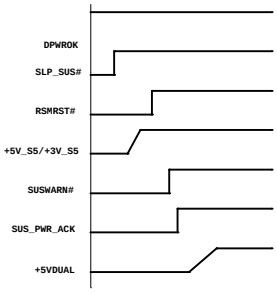
## G3 to S4/S5 Timing Diagram

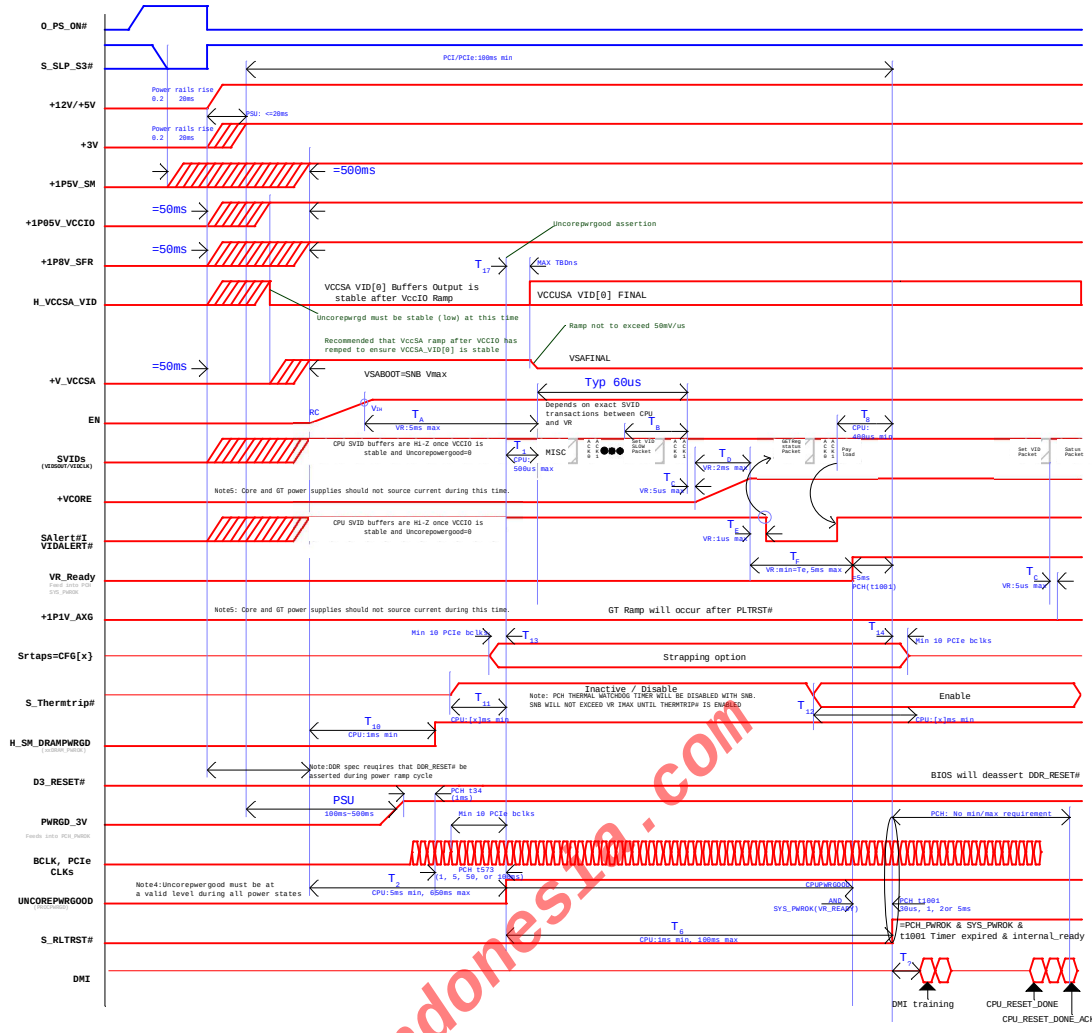



## Deep Sleep Entry




## Deep Sleep Exit






DELL INC.

Title: **Power On Sequence**

DWG NO: ***Gold Coast_MT/DT*** Rev: A00

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## RESET / Power Good MAP

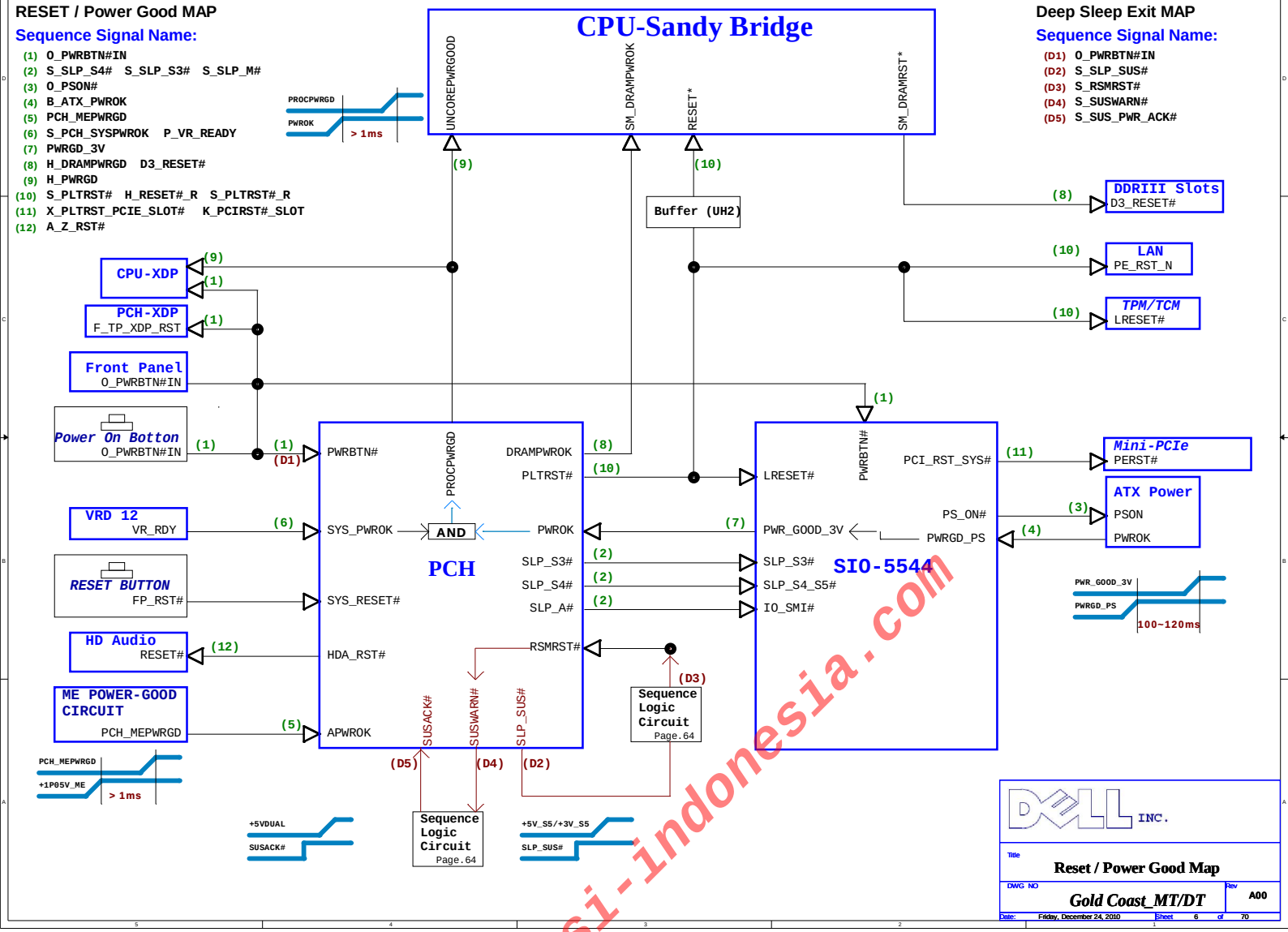
**Sequence Signal Name:**

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) S_PLTRST# H_RESET#_R S_PLTRST#_R
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#

## Deep Sleep Exit MAP

**Sequence Signal Name:**

(D1) O_PWRBTN#IN
(D2) S_SLP_SUS#
(D3) S_RSMRST#
(D4) S_SUSWARN#
(D5) S_SUS_PWR_ACK#




DELL INC.

Title: Reset / Power Good Map

DWG NO: Gold Coast_MT/DT

Rev: A00

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## IRQ Routing Table

| | INTA# | INTB# | INTC# | INTD# | IDSEL | REQn# | GNTn# |
|---|---|---|---|---|---|---|---|
| Slot3 | C | D | A | B | 18 | 0 | 0 |

## STRAPPING Table

### CPU side

| CFG[17:0] | Description | |
|---|---|---|
| [2] | PCI Express static x16 lane numbering reversal | 1: normal Default<br>0: lane numbers reversed |
| [6:5] | PCI Express Bifurcation | 00: 1x8, 2x4 PCI Express<br>01: reserved<br>10: 2x8 PCI Express<br>11: 1x16 PCI Express Default |

### Clock Gen.

| FREQ | C_CK_BSEL0 | C_CK_BSEL1 | C_CK_BSEL2 |
|---|---|---|---|
| 100 | 1 | 0 | 1 |
| 133 | 1 | 0 | 0 |

Default

| PIN NAME | NET | | Strapping description |
|---|---|---|---|
| PCI2/TME (PIN4) | C_CK505_33M_PCI2 | 1 | Overclocking DISABLED DEFAULT |
| | | 0 | Overclocking ENABLED |
| PCI4/SRC5_EN (PIN6) | C_CK505_33M_PCI4 | 1 | SRC5 DEFAULT |
| | | 0 | CPU_STOP# and PCI_STOP# |
| PCIF5/ITP_EN (PIN7) | C_CK505_33M_PCI5 | 1 | CPU_ITP |
| | | 0 | SRC8 DEFAULT |
| PCI3/CFGP (PIN5) | C_CK505_33M_PCI3 | Low | See CFG Table DEFAULT<br>(Set SATA and SRC come from PLL4) |
| | | Mid | See CFG Table |
| | | High | See CFG Table |

## SIO SMSC5544

| PIN NAME | NET | | Strapping description |
|---|---|---|---|
| GP070 / PWM4 (PIN127) | O_SPEAKER | 1 | Diag_En Disable |
| | | 0 | Diag_En Enable DEFAULT |
| DTR1# [TEST_EN] /GP051 (PIN104) | O_DTR1#_R | 1 | PE BOOT Loader Strap (DTR1#)= Load from SPI |
| | | 0 | PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT |

## PCH

**On-Die PLL Voltage Regulator Voltage Select**

| HDA_SYNC | Description |
|---|---|
| High | 1.5V |
| Low | 1.8V DEFAULT |

**On-Die PLL Voltage Regulator**

| GPIO28 (IN-PU) | Description |
|---|---|
| High | Regulator is enabled. DEFAULT |
| Low | Regulator is disabled. |

**Topblock Swap Mode**

| GNT3#/GPIO55 (IN-PU) | Description |
|---|---|
| High | Topblock swap mode: Disable DEFAULT |
| Low | Topblock swap mode: Enable |

**No Reboot Mode**

| SPKR (IN-PD) | Description |
|---|---|
| High | No reboot mode: Enable |
| Low | No reboot mode: Disable DEFAULT |

**Integrated 1.05V VRM**

| INTVRMEN | Description |
|---|---|
| High | Integrated 1.05V VRM: Enable DEFAULT |
| Low | Integrated 1.05V VRM: Disable |

**TLS Confidentiality**

| GPIO15 (IN-PD) | Description |
|---|---|
| High | ME Crypto TLS cipher suite with confidentiality |
| Low | ME Crypto TLS cipher suite with no confidentiality DEFAULT |

**Flash Descriptor Override Strap**

| HDA_SDO | Description |
|---|---|
| High | Flash descriptor security will be override |
| Low | Disable ME in Manufacturing Mode DEFAULT |

**DMI Rx Termination Voltage**

| SPI_MOSI (IN-PD) | Description |
|---|---|
| Low | DMI Rx Termination Voltage DEFAULT |

**DMI Termination Voltage**

| NV_CLE (IN-PU) | Description |
|---|---|
| High | DMI and FDI Tx/Rx Termination Voltage DEFAULT |

**Boot BIOS Destination Selection**

| GNT1# (IN-PU) | SATA1GP/GP19 (IN-PU) | Description |
|---|---|---|
| Low | Low | Flash cycle routed to LPC |
| High | Low | Flash cycle routed to PCI |
| Low | High | Flash cycle routed to NAND |
| High | High | Flash cycle routed to SPI DEFAULT |

**Deep S4/S5 Well on-die Voltage Regulator Enable**

| DSWVRMEN | Description |
|---|---|
| High | Enable DEFAULT |
| Low | Disable |

**Digital Port C Strap**

| DDPC_CTRLDATA | Description |
|---|---|
| High | Configure Port C DEFAULT |
| Low | Disable |



DELL INC.

Title: GPIO/IRQ/IDSEL Table

DWG NO: Gold Coast_MT/DT

Rev: A00

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## PCH GPIO Summary

| GPIO | Type | Power Well | Default | IN-PU/PD | EX-PU/PD | Schematic Usage |
|---|---|---|---|---|---|---|
| GPIO[0] | I/O | Core | GPI | -- | 10k pull-up to +3V | S_PECI_REQ# |
| GPIO[1] | I/O | Core | GPI | 20K IN-PU (only on TACH1) | 10k pull-up to +3V (dummy)<br>1k pull-down to GND | S_GPI_CHASSIS_ID0 |
| GPIO[2] | I/OD | Core | GPI | -- | 8.2k pull-up to +3V | PCIE_MINI_CPUSB_DETECT# |
| GPIO[3] | I/OD | Core | GPI | -- | -- | V_DDSP_C_HPD |
| GPIO[4] | I/OD | Core | GPI | -- | 8.2k pull-up to +3V | V_GPI_VGA_CBL_DET# |
| GPIO[5] | I/OD | Core | GPI | -- | 8.2k pull-up to +3V | PCIE_MINI_CPPE_DETECT# |
| GPIO[6] | I/O | Core | GPI | 20K IN-PU (only on TACH2) | 10k pull-up to +3V | S_GPI_PCH_HS_DET# |
| GPIO[7] | I/O | Core | GPI | 20K IN-PU (only on TACH3) | 10k pull-up to +3V (dummy)<br>220 pull-down to GND | S_GPI_SKU2 |
| GPIO[8] | I/O | Suspend | GPO | 20K IN-PU | -- | S_TP_GP8 |
| GPIO[9] | I/O | Suspend | Native | -- | 8.2k pull-up to +3V_S5 (dummy) | U_USB_OC_R_#5 |
| GPIO[10] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | X_WLAN_WAKE# |
| GPIO[11] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | X4_WAKE# |
| GPIO[12] | I/O | Suspend | Native | -- | 10k pull-up to +3V_LAN<br>10k pull-down to GND (dummy) | L_LAN_DISABLE# |
| GPIO[13] | I/O | Suspend | GPI | -- | 10k pull-up to +3V_S5 | X1_WAKE# |
| GPIO[14] | I/O | Suspend | Native | -- | 8.2k pull-up to +3V_S5 | GPIO_WLOM |
| GPIO[15] | I/O | Suspend | GPO | 20K IN-PD | 1k pull-up to +3V_S5 (dummy) | S_PCH_GP15 |
| GPIO[16] | I/O | Core | GPI | -- | 10k pull-up to +3V<br>10k pull-down to GND (dummy) | H_SKTOCC_R_# |
| GPIO[17] | I/O | Core | GPI | 20K IN-PU (only on TACH0) | 10k pull-up to +3V (dummy)<br>1k pull-down to GND | S_GPI_CHASSIS_ID1 |
| GPIO[19] | I/O | Core | GPI | 20K IN-PU | 1k pull-up to +3V (dummy)<br>1k pull-down to GND (dummy) | S_SATA1GP |
| GPIO[20] | I/O | Core | Native | -- | 10k pull-up to +3V<br>10k pull-down to GND (dummy) | S_FLEXBAY_HDR_CBL_DET# |
| GPIO[21] | I/O | Core | GPI | -- | 10k pull-up to +3V (dummy)<br>10k pull-down to GND | S_GPI_BRD_REV0 |
| GPIO[22] | I/O | Core | GPI | -- | 1k pull-up to +3V<br>4.7k pull-down to GND (dummy) | S_PCH_CONFIG_JUMPER |
| GPIO[23] | I/O | Core | Native | 20K IN-PU | 10k pull-up to +3V (dummy) | L_DRQ1# |
| GPIO[24] | I/O | Suspend | GPO | -- | 100k pull-up to +3V_S5 | H_SKTOCC# |
| GPIO[27] | I/O | Deep Sleep | GPI | 20K IN-PU | 10k pull-up to +3V_DUAL<br>1k pull-down to GND (dummy) | S_GP27_PD |
| GPIO[28] | I/O | Suspend | GPO | 20K IN-PU | 10k pull-up to +3V_S5<br>1k pull-down to GND (dummy) | S_PCH_GP28_PU |
| GPIO[29] | I/O | Suspend | Native | -- | 1k pull-up to +3V_S5 (dummy) | S_SLP_LAN# |
| GPIO[30] | I/O | Deep Sleep | Native | -- | 10k pull-up to +3V_DUAL (dummy)<br>1k pull-down to GND (dummy) | S_SUSWARN# |
| GPIO[31] | I/O | Deep Sleep | GPI | TBD IN-PD | 8.2k pull-up to +3V_DUAL | S_PSWD_CLR |
| GPIO[32] | I/O | Core | GPO | -- | 10k pull-up to +3V (dummy)<br>220 pull-down to GND | S_GPI_SKU0 |
| GPIO[33] | I/O | Core | GPO | -- | --- | -- |
| GPIO[34] | I/O | Core | GPI | -- | 10k pull-up to +3V | PCH_GPIO34 |
| GPIO[35] | I/O | Core | GPO | -- | 10k pull-up to +3V (dummy)<br>220 pull-down to GND | S_GPI_SKU1 |
| GPIO[36] | I/O | Core | GPI | 20K IN-PD | --- | S_PCH_GP36 |
| GPIO[37] | I/O | Core | GPI | 20K IN-PD | --- | S_PCH_GP37 |
| GPIO[38] | I/O | Core | GPI | -- | 10k pull-up to +3V (dummy)<br>10k pull-down to GND | S_GPI_CHASSIS_ID2 |
| GPIO[39] | I/O | Core | GPI | -- | 10k pull-up to +3V | A_FP_PRES# |
| GPIO[40] | I/O | Suspend | Native | -- | --- | U_USB_OC_R_#1 |
| GPIO[41] | I/O | Suspend | Native | -- | --- | U_USB_OC_R_#2 |
| GPIO[42] | I/O | Suspend | Native | -- | --- | U_USB_OC_R_#3 |
| GPIO[43] | I/O | Suspend | Native | -- | 8.2k pull-up to +3V_S5 (dummy) | U_USB_OC_R_#4 |
| GPIO[44] | I/O | Suspend | Native | 20K IN-PU | 10k pull-up to +3V_S5<br>10k pull-down to GND (dummy) | S_INTRUD_CBL_DET# |
| GPIO[45] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5<br>10k pull-down to GND (dummy) | O_COM_SER2_DET# |
| GPIO[46] | I/O | Suspend | Native | 20K IN-PU | 10k pull-up to +3V_S5 (dummy)<br>1k pull-down to GND | S_GPI_BRD_REV1 |
| GPIO[48] | I/O | Core | GPI | -- | 10k pull-up to +3V | S_GPIO48_PU |
| GPIO[49] | I/O | Core | GPI | -- | 8.2k pull-up to +3V | TMIN_SHIFT |
| GPIO[50] | I/O | Core | Native | -- | 8.2k pull-up to +3V | K_REQ#1 |
| GPIO[51] | I/O | Core | Native | 20K IN-PU | 1k pull-up to +3V (dummy)<br>1k pull-down to GND (dummy) | K_GNT#1 |
| GPIO[52] | I/O | Core | Native | -- | 8.2k pull-up to +3V | K_REQ#2 |
| GPIO[53] | I/O | Core | Native | 20K IN-PU | 1k pull-down to GND (dummy) | K_GNT#2 |
| GPIO[54] | I/O | Core | Native | -- | 8.2k pull-up to +3V | K_REQ#3 |
| GPIO[55] | I/O | Core | Native | 20K IN-PU | 1k pull-down to GND (dummy) | K_GNT#3 |
| GPIO[57] | I/O | Suspend | GPI | -- | 10k pull-up to +3V_S5 (dummy)<br>47k pull-down to GND | S_GPIO57_PD |
| GPIO[58] | I/O | Suspend | Native | | 10k pull-up to +3V_S5 | S_SMLINK1_CLK |
| GPIO[59] | I/O | Suspend | Native | -- | --- | U_USB_OC_R_#0 |
| GPIO[60] | I/O | Suspend | Native | -- | 2.2k pull-up to +3V_S5 | GPIO_WIRELESS_DISABLE# |
| GPIO[61] | I/O | Suspend | Native | -- | 8.2k pull-up to +3V_S5 (dummy) | S_LPCPD# |
| GPIO[62] | I/O | Suspend | Native | -- | -- | S_SUSCLK |
| GPIO[63] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_PCIAUX_GATE |
| GPIO[64] | I/O | Core | Native | 20K IN-PD | --- | S_TP_CLKOUTFLEX0 |
| GPIO[65] | I/O | Core | Native | 20K IN-PD | --- | C_14M_SIO_R |
| GPIO[66] | I/O | Core | Native | 20K IN-PD | --- | S_TP_CLKOUTFLEX2 |
| GPIO[67] | I/O | Core | Native | 20K IN-PD | --- | C_14M_TPM_R |
| GPIO[68] | I/O | Core | GPI | 20K IN-PU (only on TACH4) | 10k pull-up to +3V (dummy)<br>220 pull-down to GND | S_GPI_BRD_REV2 |
| GPIO[69] | I/O | Core | GPI | 20K IN-PU (only on TACH5) | 10k pull-up to +3V | O_PRT_DET# |
| GPIO[70] | I/O | Core | Native | 20K IN-PU (only on TACH6) | 8.2k pull-up to +3V | S_FP_CHAS_DET# |
| GPIO[71] | I/O | Core | Native | 20K IN-PU (only on TACH7) | 10k pull-up to +3V | -- |
| GPIO[72] | I/O | Suspend | Native (Mobile Only) | 20K IN-PU | 10k pull-up to +3V_S5 | S_PCH_GP72_PU |
| GPIO[74] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_MFG_MODE_OR |
| GPIO[75] | I/O | Suspend | Native | -- | 10k pull-up to +3V_S5 | S_SMLINK1_DATA |

| GPIO | PIN NAME | Power well | Buffer Type | EX-PU/PD | Signal Name |
|---|---|---|---|---|---|
| GP000 | (DAC_LED3#) GP000 | VTR | IO | NA | O_DAC_LED3# |
| GP001 | (DAC_LED1#) GP001 | VTR | IO | NA | O_DAC_LED1# |
| GP002 | (DAC_LED2#) GP002 | VTR | IO | NA | O_DAC_LED2# |
| GP003 | (DAC_LED4#) GP003 | VTR | IO | NA | O_DAC_LED4# |
| GP004 | GP004 | VTR | IO | NA | NC |
| GP005 | (H_CPURST#) GP005 / PECI_REQUEST# | VTR | IO/OD | 1.5k pull-up to +3V | O_PECI_REQ# |
| GP006 | YELLOW## / GP006 | VTR | OA0 | NA | O_YELLOW## |
| GP007 | GREEN## / GP007 | VTR | OA0 | NA | O_GREEN# |
| GP010 | SMBDAT2 / GP010 | VTR | IO/OA0 | 8.2k pull-up to +3V_DUAL(dummy) | S_SMLINK1_DATA_R |
| GP011 | SMBCLK2 / GP011 | VTR | IO/OA0 | 8.2k pull-up to +3V_DUAL (dummy) | S_SMLINK1_CLK_R |
| GP012 | GP012 | VTR | IO | 8.2k pull-up to +3V_DUAL | SPI_DI |
| GP013 | GP013 | VTR | IO | NA | NC |
| GP014 | (TMIN_SHIFT) GP014 | VTR | IO | 8.2k pull-up to +3V | TMIN_SHIFT |
| GP015 | PWRBTN# / GP015 | VTR | I/O | 1k pull-up to +3V_DUAL | O_PWRBTN#IN |
| GP016 | PROCHOT_IN##/PROCH0T_OUT##/GP016 | VTR | I/OD/IOD | 51ohm pull-up to +1P05V_VCCIO | H_PROCHOT# |
| GP017 | TACH1 / GP017 | VTR | I/O | 1k pull-up to +3V | O_SEN_CPUFAN |
| GP020 | TACH2 / GP020 | VTR | I/O | 1k pull-up to +3V | O_SEN_CHAFAN |
| GP021 | TACH3 / GP021 | VTR | I/O | NA | NC |
| GP022 | PWM1 / GP022 | VTR | OD/A0 | 4.7k pull-up to +3V | O_CPUFAN_PWM |
| GP023 | PWM2 / GP023 | VTR | OD/A0 | 4.7k pull-up to +3V | O_CHAFAN_PWM |
| GP024 | PWM3 / GP024 | VTR | OD/A0 | NA | NC |
| GP025 | (FP_CBL_DET#) GP025 | VTR | IO | 8.2k pull-up to +3V_S5 | O_FP_CBL_DET# |
| GP026 | PCI_RST_SYS# / GP026 | VTR | OA0 | NA | X_PLTRST_PCIE_SLOT# |
| GP027 | PCI_RST_SLOTS# / GP027 | VTR | OA0 | NA | H_RESET# |
| GP030 | PS_ON## / GP030 | VTR | OD/A0 | 4.7k pull-up to +5VSB | O_PSON# |
| GP031 | (PC_SPKR_DET) GP031 | VTR | IO | 8.2k pull-up to +3V_DUAL | O_AUD_PCSPKR_DET# |
| GP032 | GP032 | VTR | IO | NA | NC |
| GP033 | PWR_GOOD_3V / GP033 | VTR | OA0 | NA | PWRGD_3V |
| GP034 | RSMRST## GP034 | VTR | OA0 | 1.5k pull-down to GND | O_RSMRST## |
| GP035 | GP035 | VTR | IO | 8.2k pull-up to +3V_DUAL | O_BC_CLK |
| GP036 | GP036 / SMB_CLK1 | VTR | IO/OD | 8.2k pull-up to +3V_DUAL (dummy) | S_SMBCLK_PCI_R |
| GP040 | GP040 / SMB_DAT1 | VTR | IO/OD | 8.2k pull-up to +3V_DUAL (dummy) | S_SMBDATA_PCI_R |
| GP041 | GP041 / IO_PME# | VTR | IO/OD | 1.5k pull-up to +3V_S5 | O_IO_PME# |
| GP042 | GP042 / DRVDEN0 | VTR | IO/O | 100k pull-up to +3V_DUAL(dummy | T_ESATA_DET# |
| GP043 | DCD1# / GP043 / MCDAT | VTR | I/O/O | NA | O_DCD1#_R |
| GP044 | DSR1# / GP044 / MCCLK | VTR | I/O/O | NA | O_DSR1#_R |
| GP045 | RXD1 / GP045 | VTR | I/O | NA | O_RXD1_R |
| GP046 | RTS1# / GP046 | VTR | OA0 | NA | O_RTS1#_R |
| GP047 | (5V_PSGNT) GP047 / TXD1 | VTR | IO/O | NA | O_TXD1_R |
| GP050 | CTS1# / GP050 | VTR | I/O | NA | O_CTS1#_R |
| GP051 | DTR1# (TEST_EN) / GP051 | VTR | OA0 | 8.2k pull-up to +3V_DUAL(dummy)<br>20k pull-down to GND | O_DTR1#_R |
| GP052 | RI1# / GP052 | VTR | I/O | NA | O_RI1#_R |
| GP053 | GP053 / DCD2# | VTR | IOI | 2.2k pull-up to +3V | O_DCD2#_R |
| GP054 | GP054 / DSR2# | VTR | IOI | 2.2k pull-up to +3V | O_DSR2#_R |
| GP055 | GP055 / RXD2 | VTR | IOI | 2.2k pull-up to +3V | O_RXD2_R |
| GP056 | (PWRG_PRSNT) GP056 / RTS2# | VTR | IO/O | 30k pull-up to +3V | O_RTS2#_R |
| GP057 | (MB_REQ_P0) GP057 / TXD2 | VTR | IO/O | 30k pull-up to +3V | O_TXD2_R |
| GP060 | GP060 / CTS2# | VTR | IOI | 2.2k pull-up to +3V | O_CTS2#_R |
| GP061 | (MEM_REQ_P0) GP061 / DTR2# | VTR | IO/O | 30K pull-up to +3V | O_DTR2#_R |
| GP062 | GP062 / RI2# | VTR | IOI | 2.2k pull-up to +3V | O_RI2#_R |
| GP063 | GP063 / KBDRST# | VTR | IO/OD | 1.5k pull-up to +3V | O_KB_RST# |
| GP064 | GP064 / A20M | VTR | IO/OD | 1.5k pull-up to +3V | O_GA20 |
| GP065 | SLP_S3# / GP065 | VTR | I/O | NA | S_SLP_S3# |
| GP066 | SLP_S4_S5# / GP066 | VTR | I/O | NA | S_SLP_S4# |
| GP067 | PWRGD_PS / GP067 | VTR | I/O | 1k pull-up to +5V | S_ATX_PWROK |
| GP070 | SPEAKER (DIAG_EN#) / GP070 | VTR | OA0 | 8.2k pull-up to +3V_DUAL(dummy)<br>8.25k pull-down to GND | O_SPEAKER |
| GP071 | (SLP_M#) GP071 / IO_SMI# | VTR | IO/OD | NA | S_SLP_M# |
| GP072 | PECI / LVSMB_CLK1 / GP072 | VTR | PECI_IO/OD/IO | 1k pull-up to +1P05V_VCCIO (dummy) | H_PECI_R |
| GP073 | PECI_READY / LVSMB_DAT1 / GP073 | VTR | PECI_I/O/OD/O | 1k pull-up to +1P05V_VCCIO | O_GP73_PU |

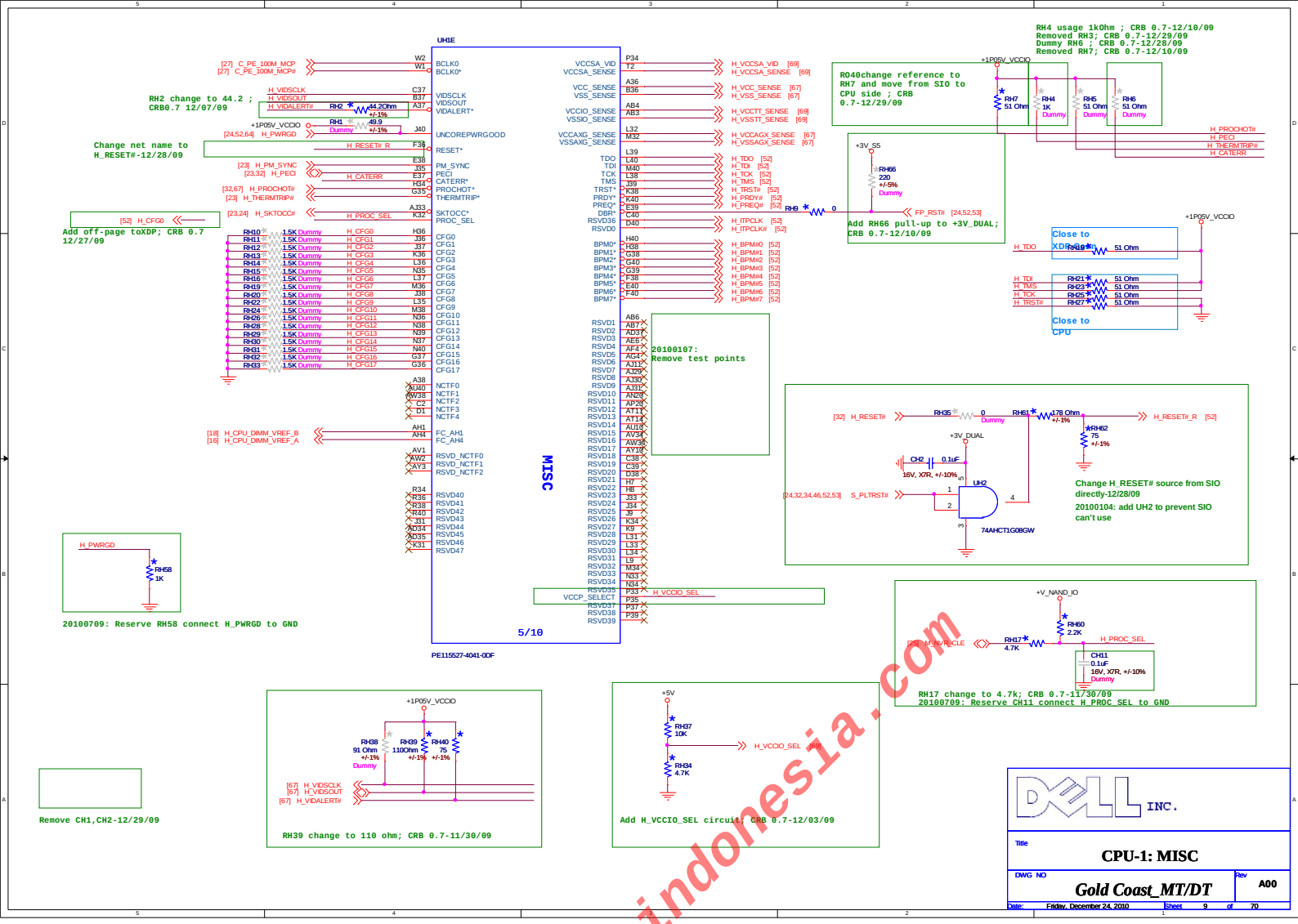


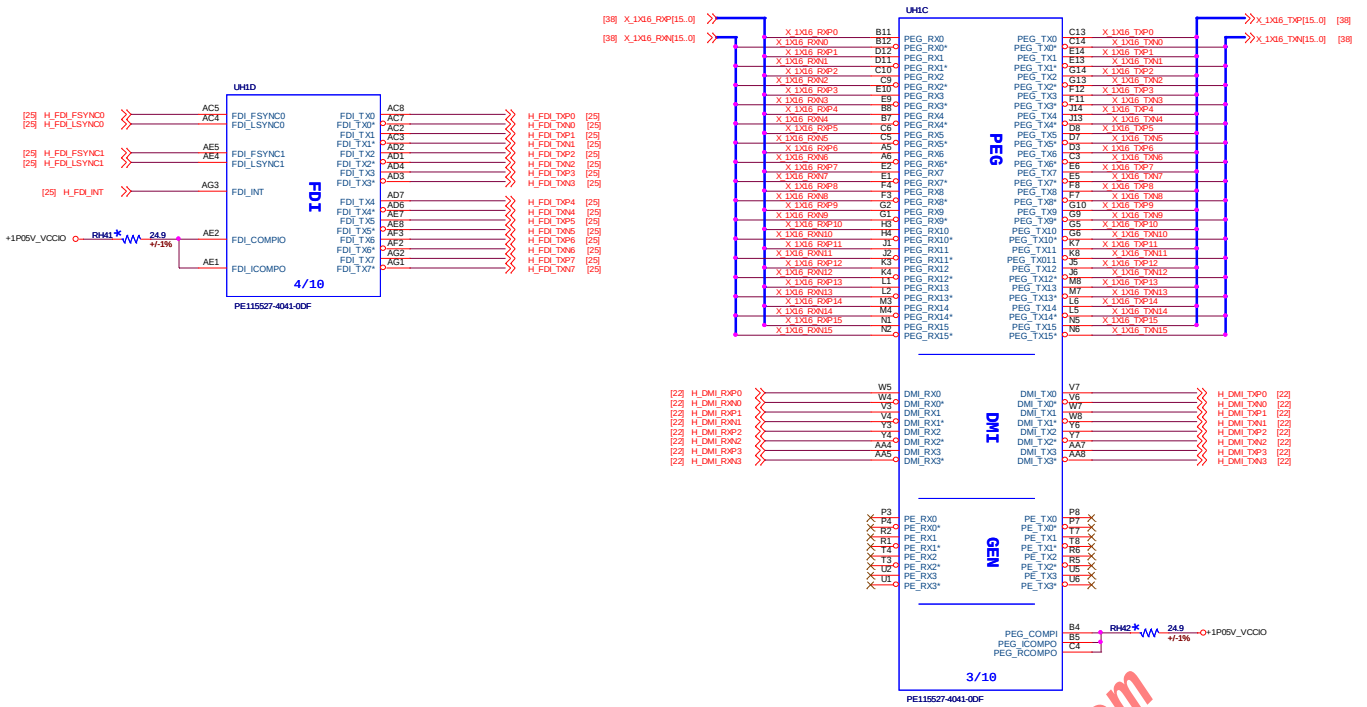
DELL INC.

Title: **GPIO Table**

DWG NO: *Gold Coast_MT/DT* Rev: A00

Date: Friday, December 24, 2010 Sheet 8 of 70







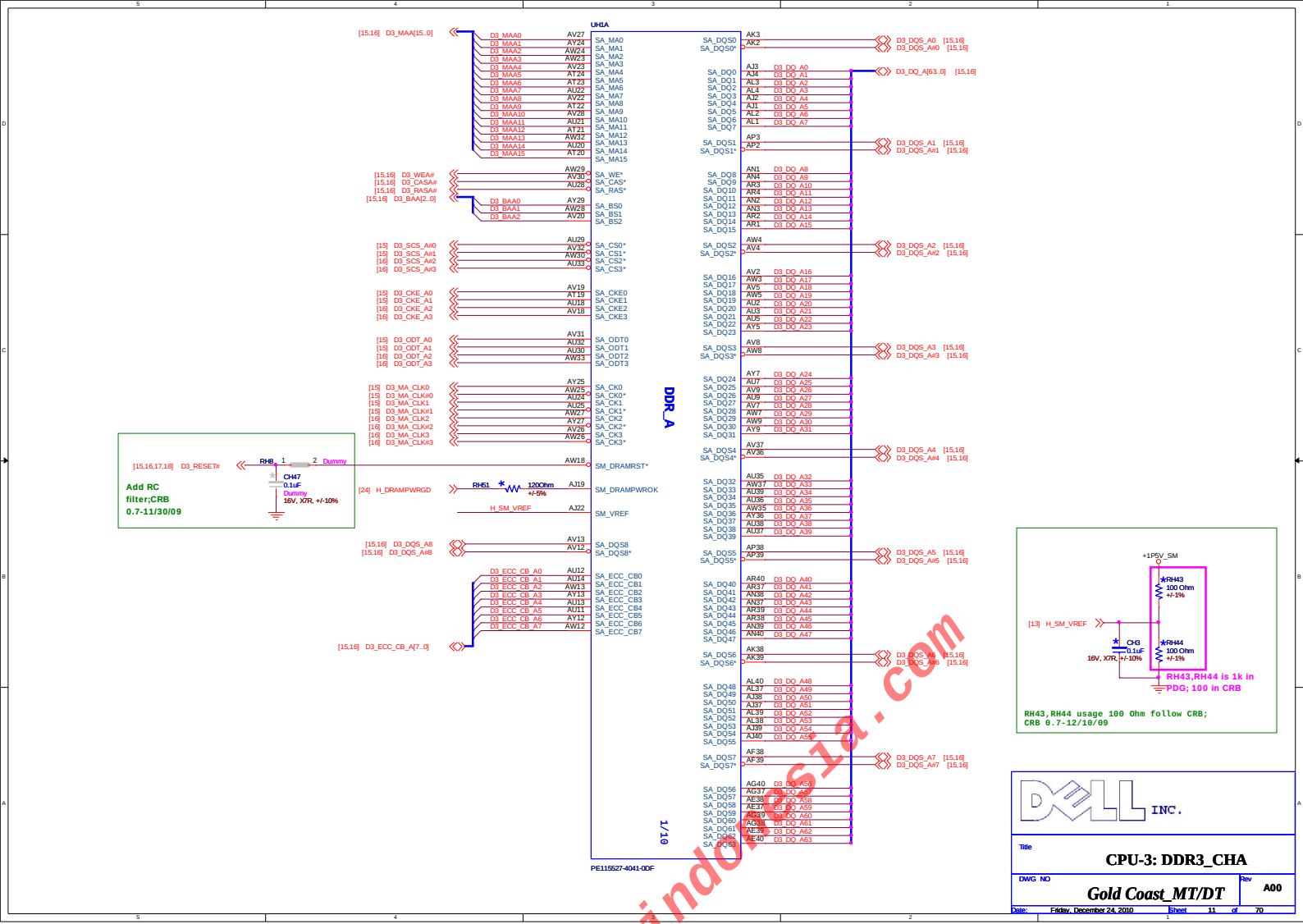

DELL INC.

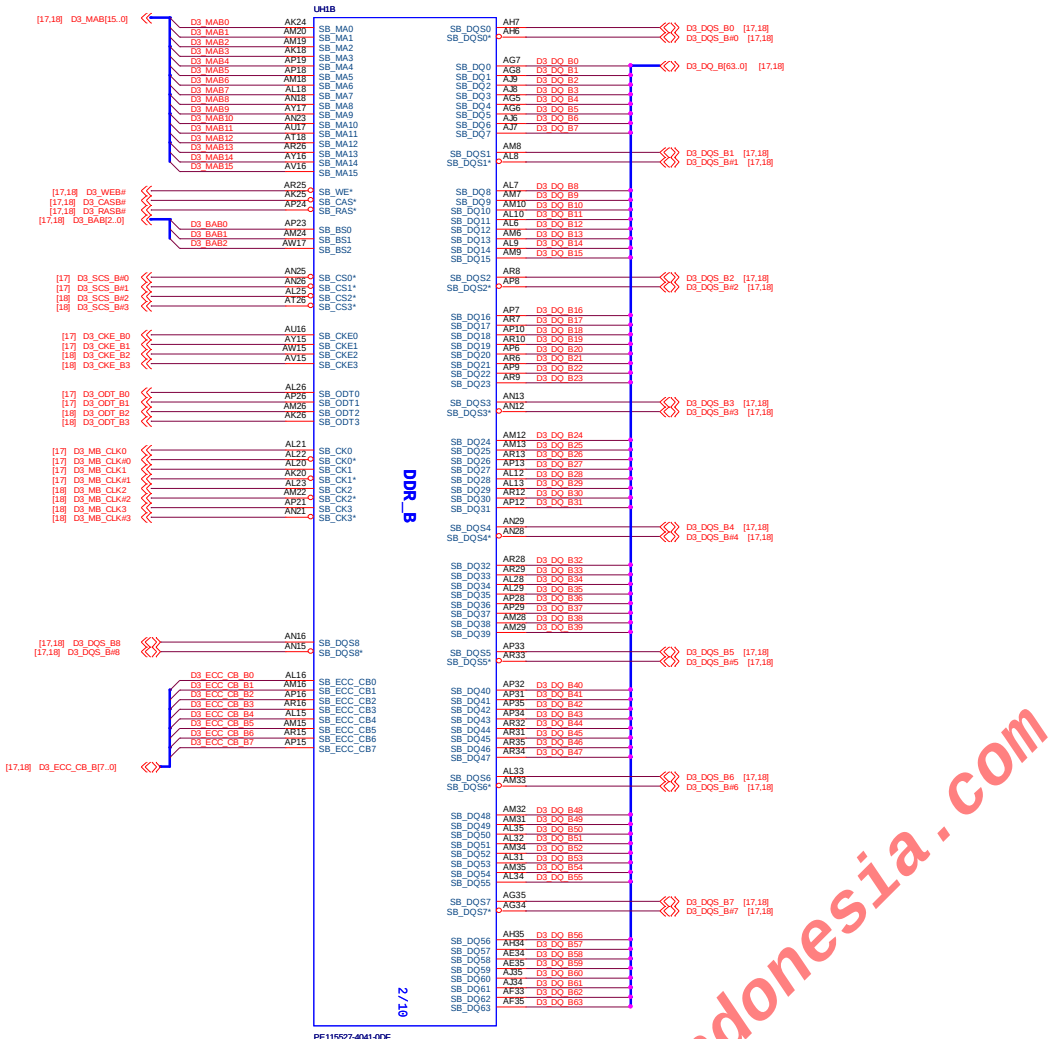
Title: CPU-2: FDI/PCIe/DMI

DWG NO: Gold Coast_MT/DT

Rev: A00

Date: Friday, December 24, 2010 Sheet 10 of 70





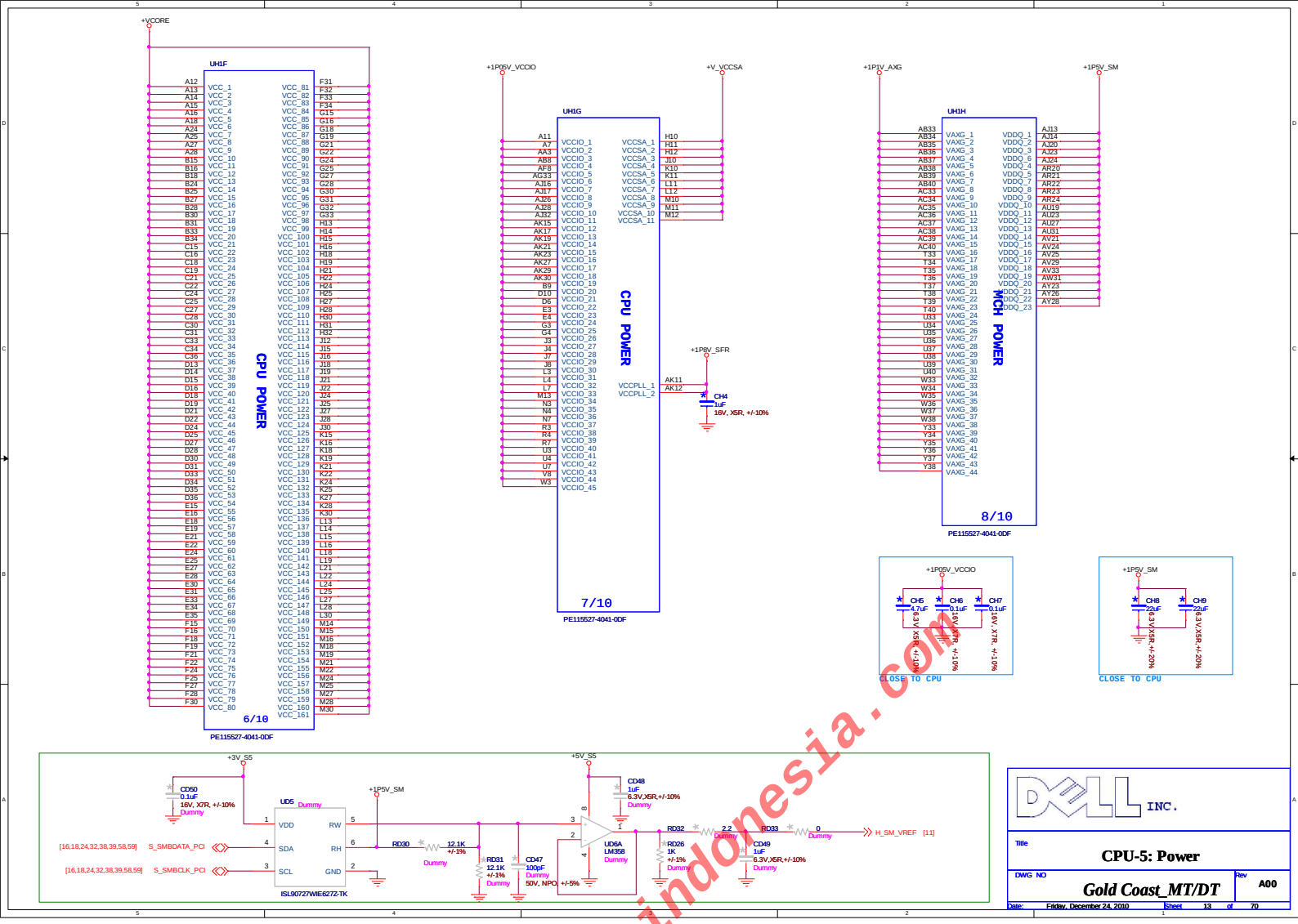

DELL INC.

Title: CPU-4: DDR3_CHB

DWG NO: Gold Coast_MT/DT

Rev: A00

Date: Friday, December 24, 2010 Sheet 12 of 70







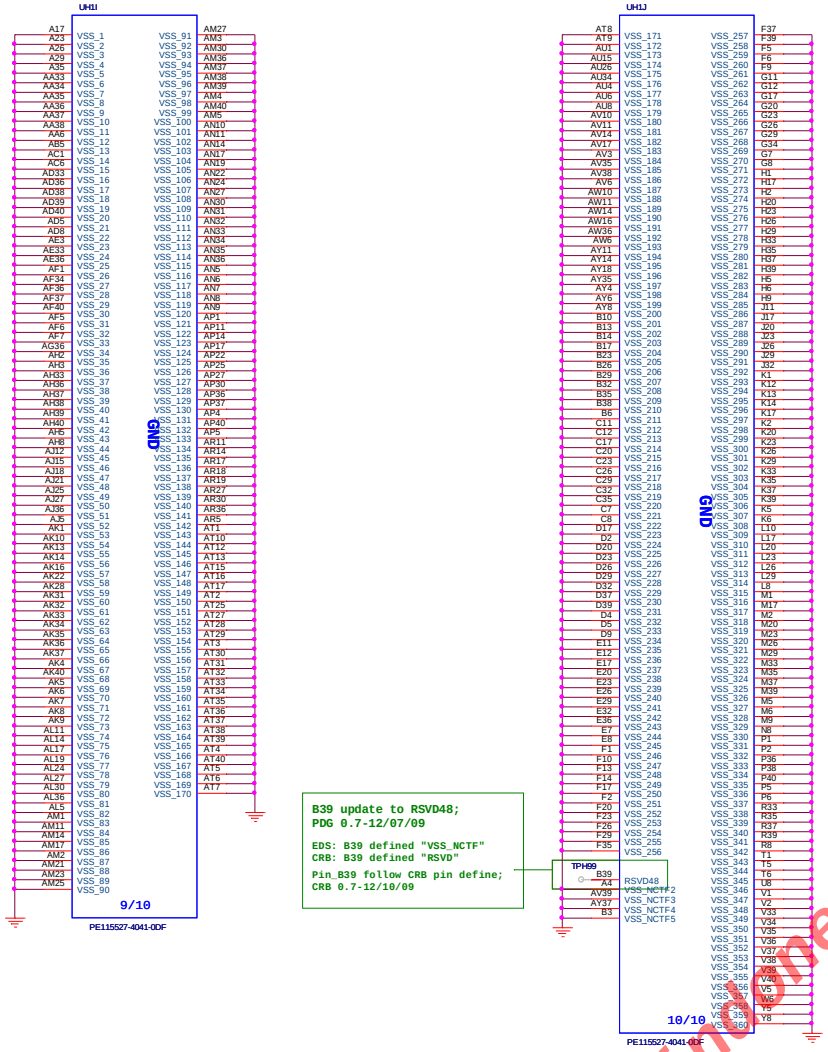
DELL INC.

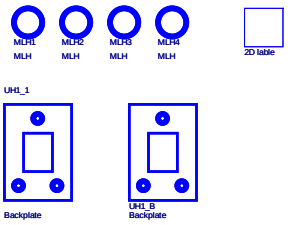
Title: **CPU-5: Power**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

Date: Friday, December 24, 2010 Sheet 13 of 70




DELL INC.

Title

**CPU-6: GND**

DWG NO

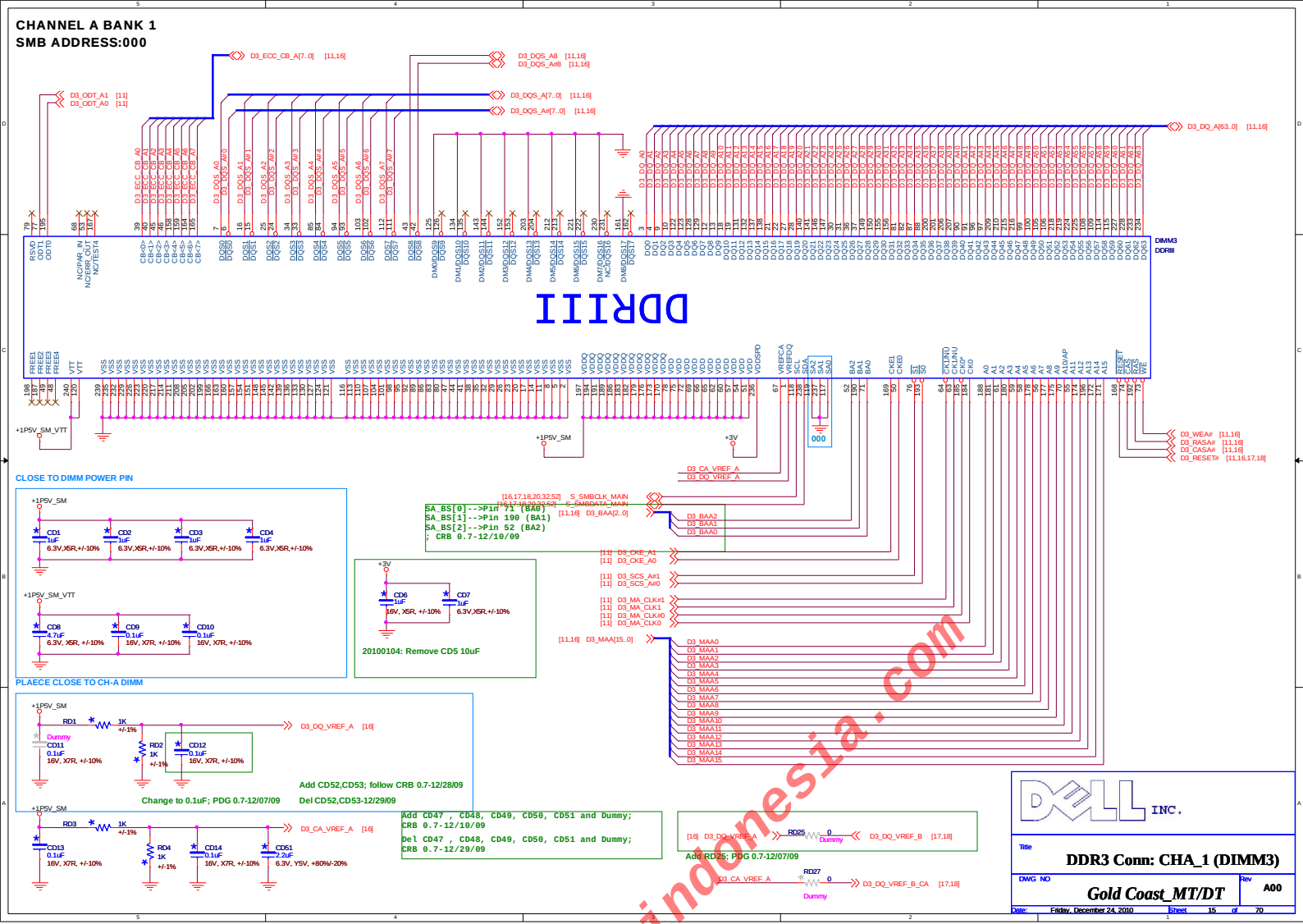
***Gold Coast_MT/DT***

Rev

**A00**

Date: Friday, December 24, 2010 Sheet 14 of 70

**CHANNEL A BANK 1**
**SMB ADDRESS:000**






DELL INC.

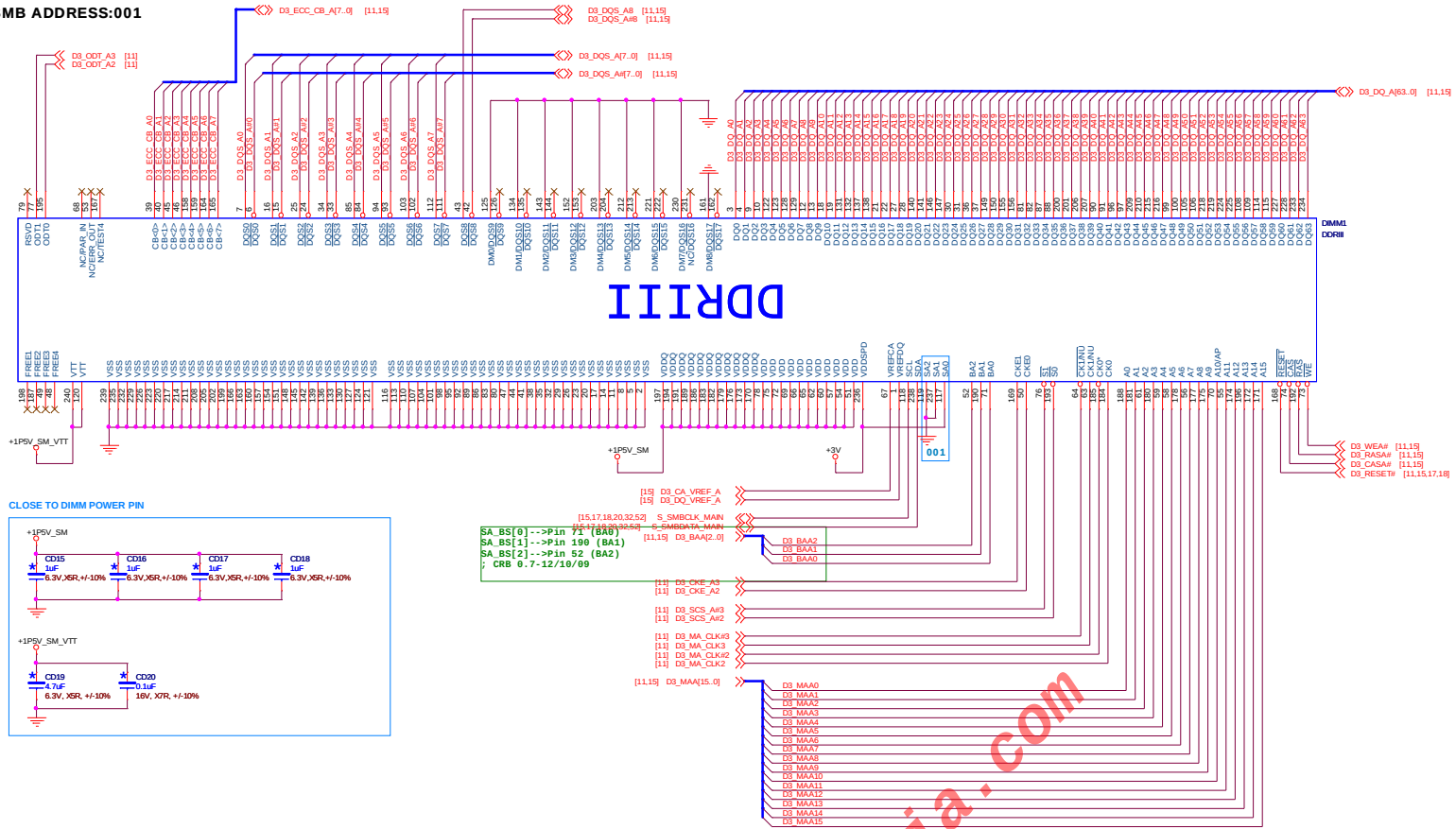
Title: **DDR3 Conn: CHA_1 (DIMM3)**

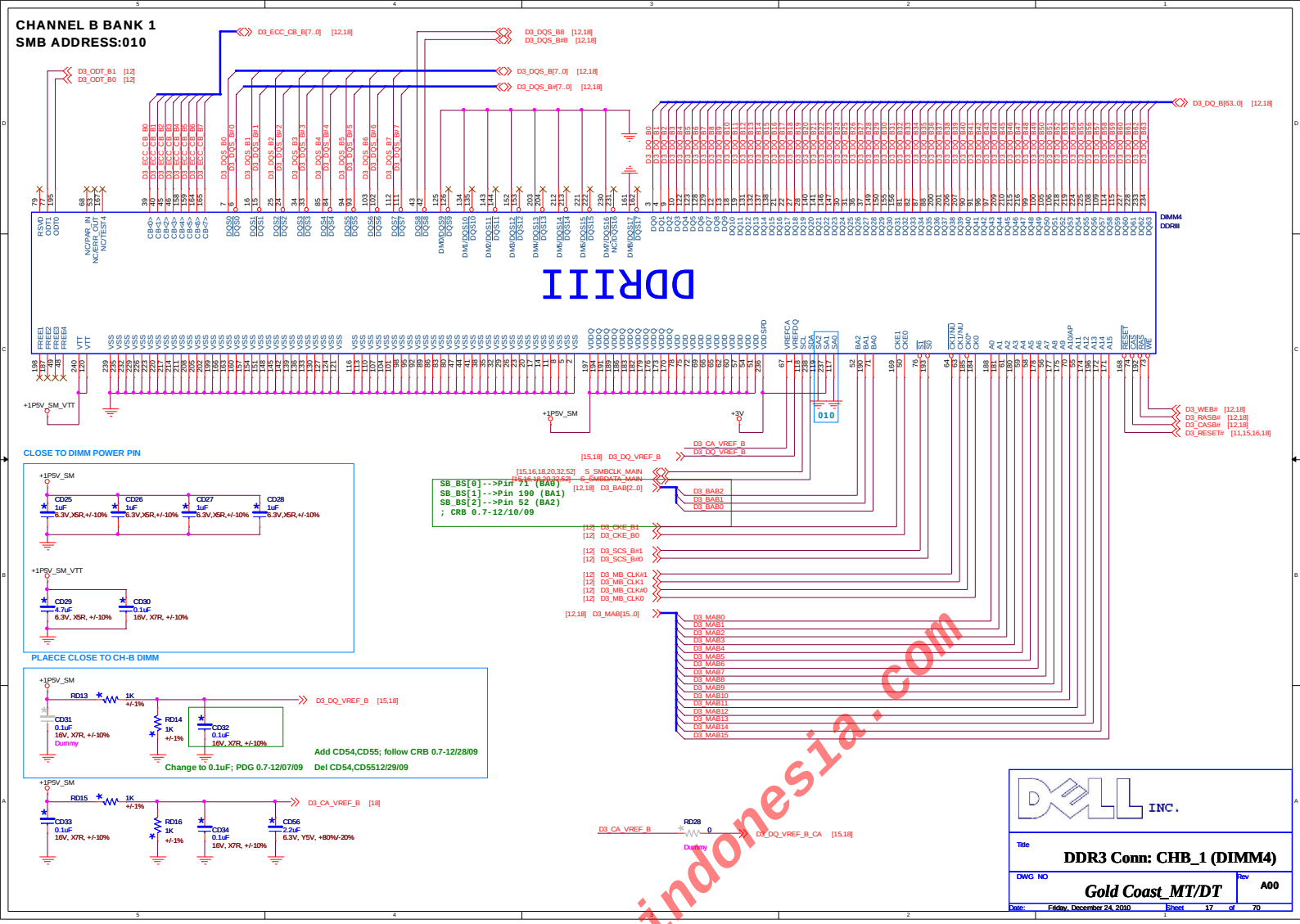
DWG NO: *Gold Coast_MT/DT*

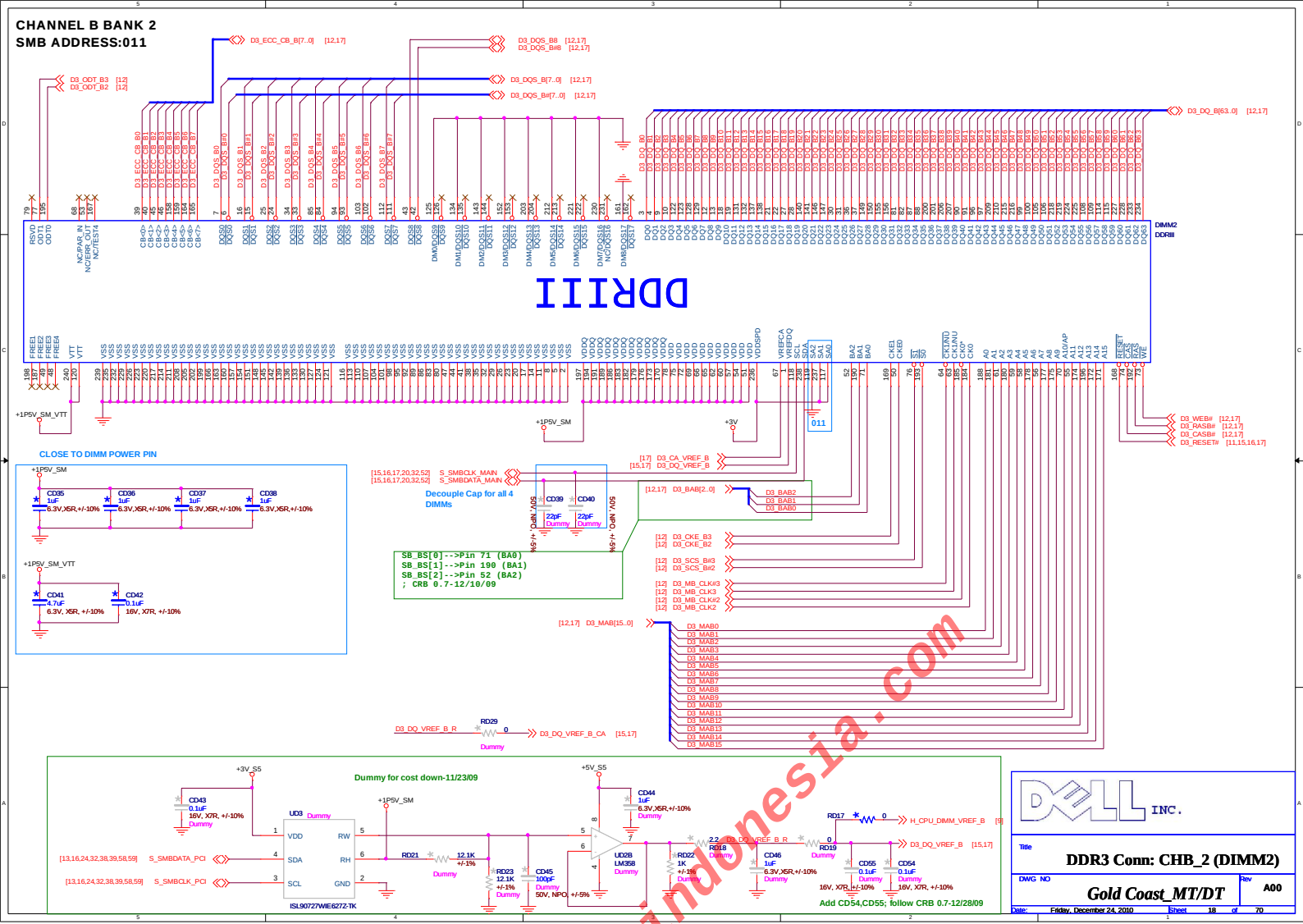
Rev: A00

Date: Friday, December 24, 2010 Sheet 15 of 70

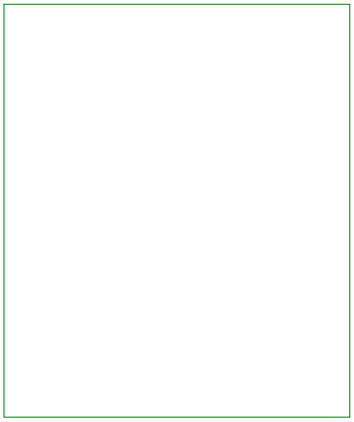
**CHANNEL A BANK 2**
**SMB ADDRESS:001**







20100106: Remove ONFI function since not support





DELL INC.

Title

**TBD**

DWG NO

***Gold Coast_MT/DT***

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**A00**

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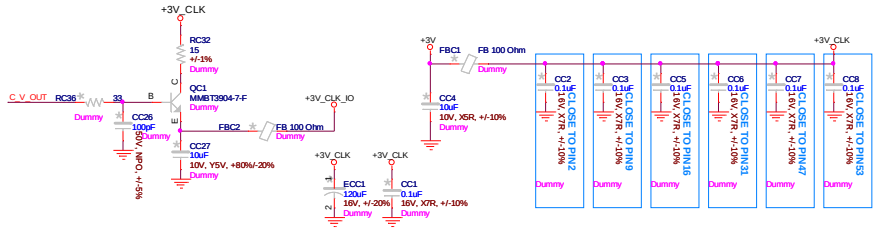
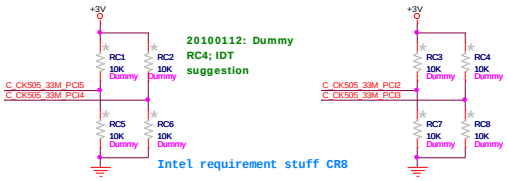


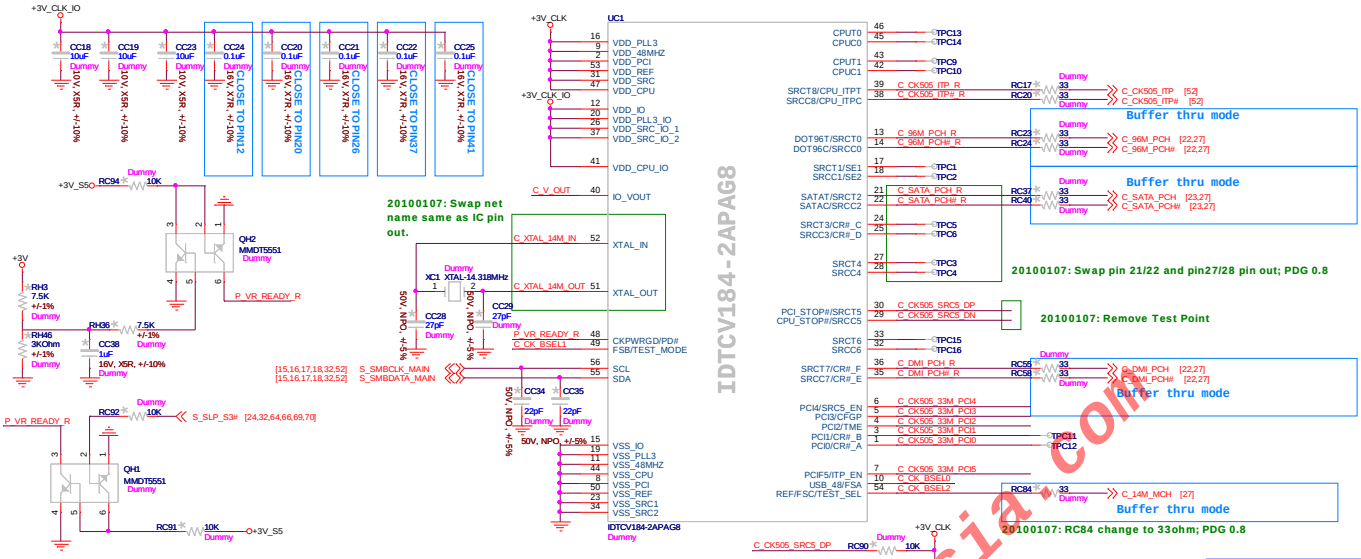

- PCI4/SRC5_EN (Pin6) Output Mode select. H=SRC5, L=CPU/PCI Stop#. Latch @ Power-On
- PCIF5/ITP_EN (Pin7) Output Mode Select. H=CPU_ITP, L= SRC8. Latch @ Power-On
- PCI2/TME (Pin4) Trust Mode Enable. H= overclocking disabled. Latch @ Power-On
- PCI3/CFGP (Pin5) Clock Config Strapping. Details refer to CLK-Gen CFG table Latch @ Power-On



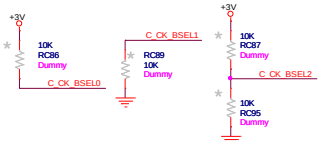

# +3V_CLK_IO

## Dummy CK505 circuit for Cost down

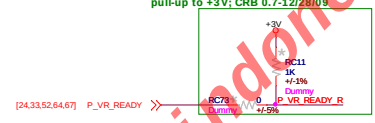
## Add CK505 buffer thru mode circuit-20091225

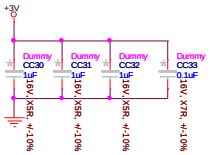



| FREQ | BSEL0 | BSEL1 | BSEL2 |
|---|---|---|---|
| 100 | 1 | 0 | 1 |
| 133 | 1 | 0 | 0 |




Dummy RC73 and add RC11 pull-up to +3V; CRB 0.7-12/28/09




DELL INC.

Title: Clock GEN

DWG NO: Gold Coast_MT/DT

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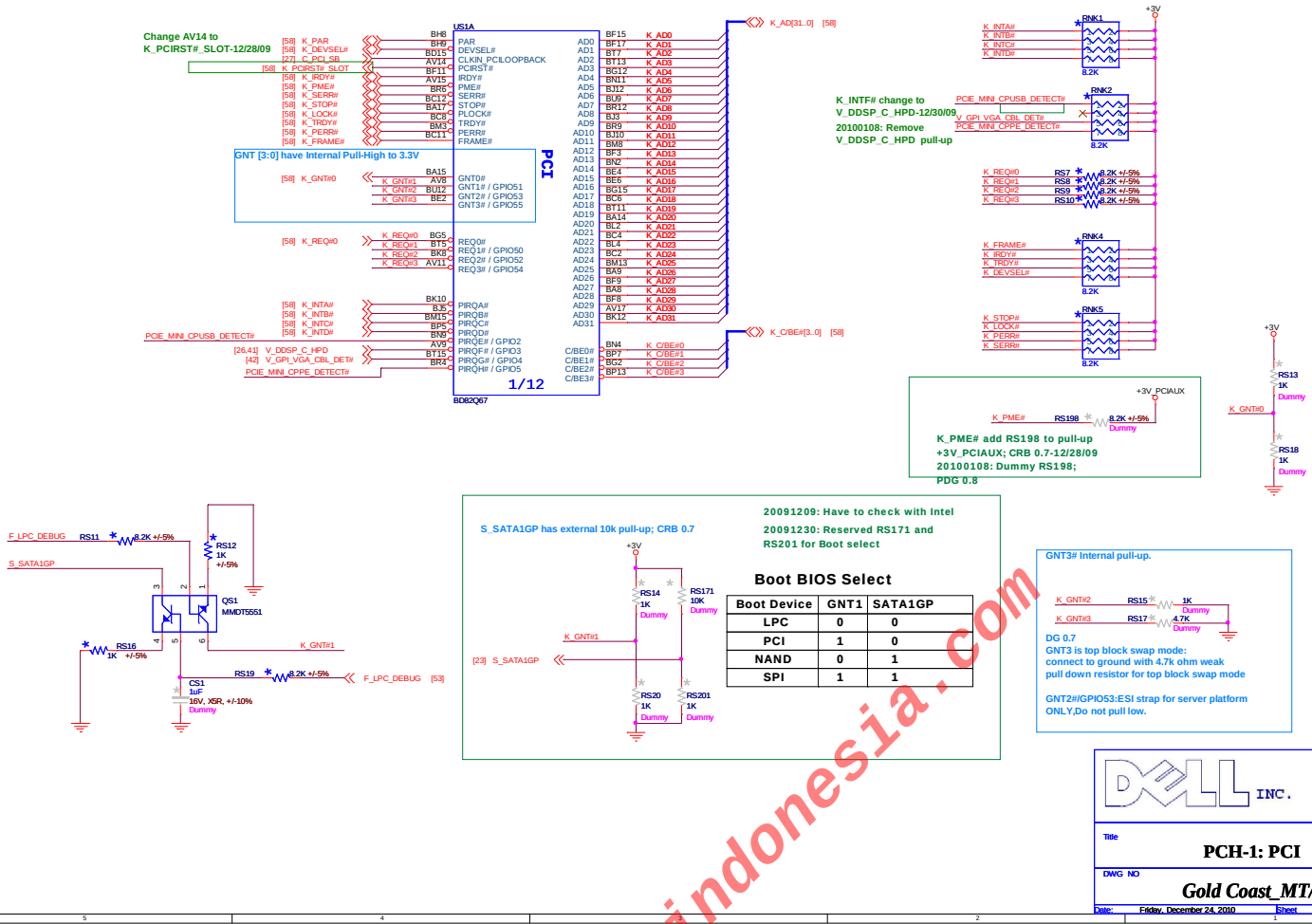
Date: Friday, December 24, 2010 Sheet 20 of 70





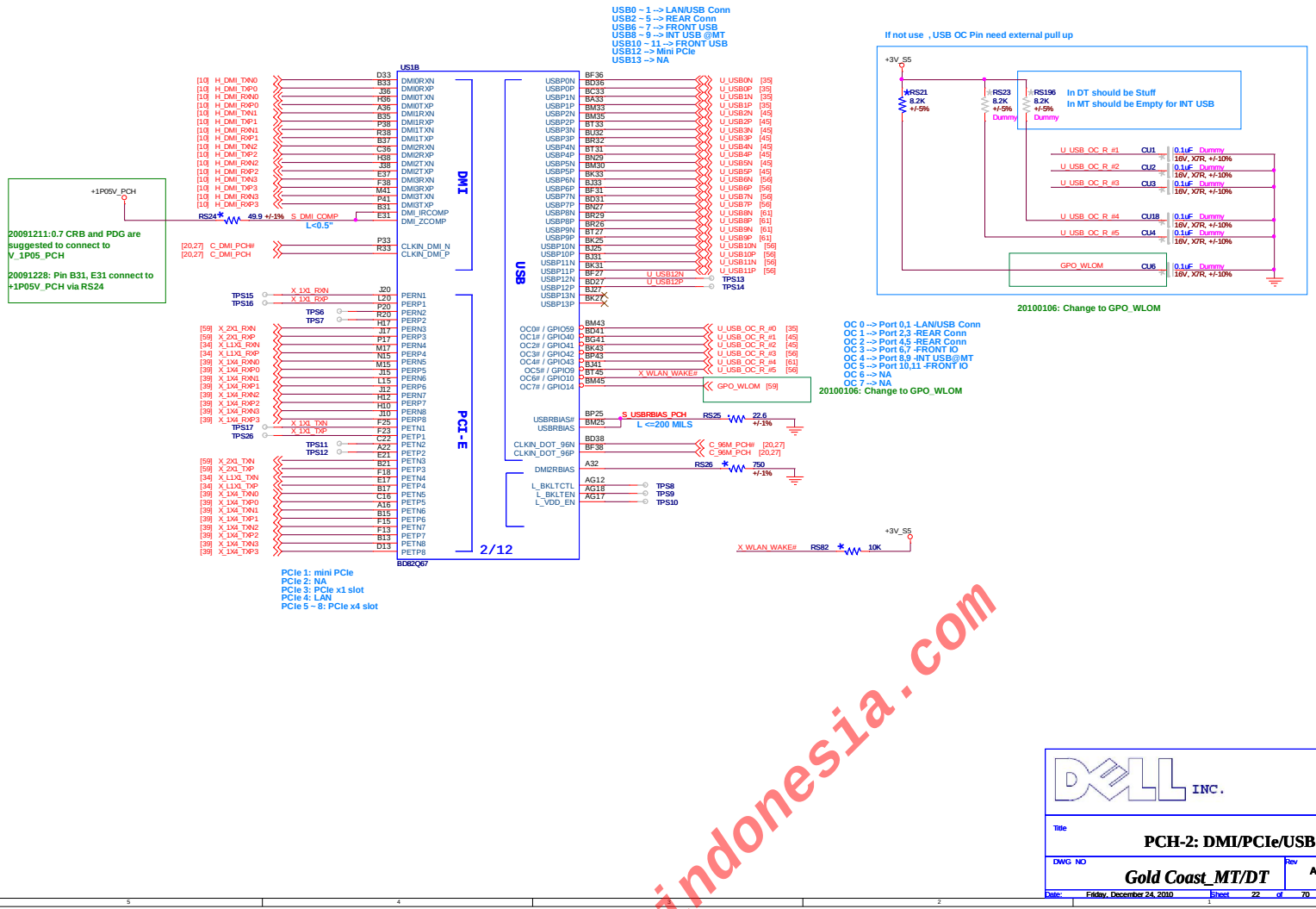

DELL INC.

Title: PCH-1: PCI

DWG NO: Gold Coast_MT/DT

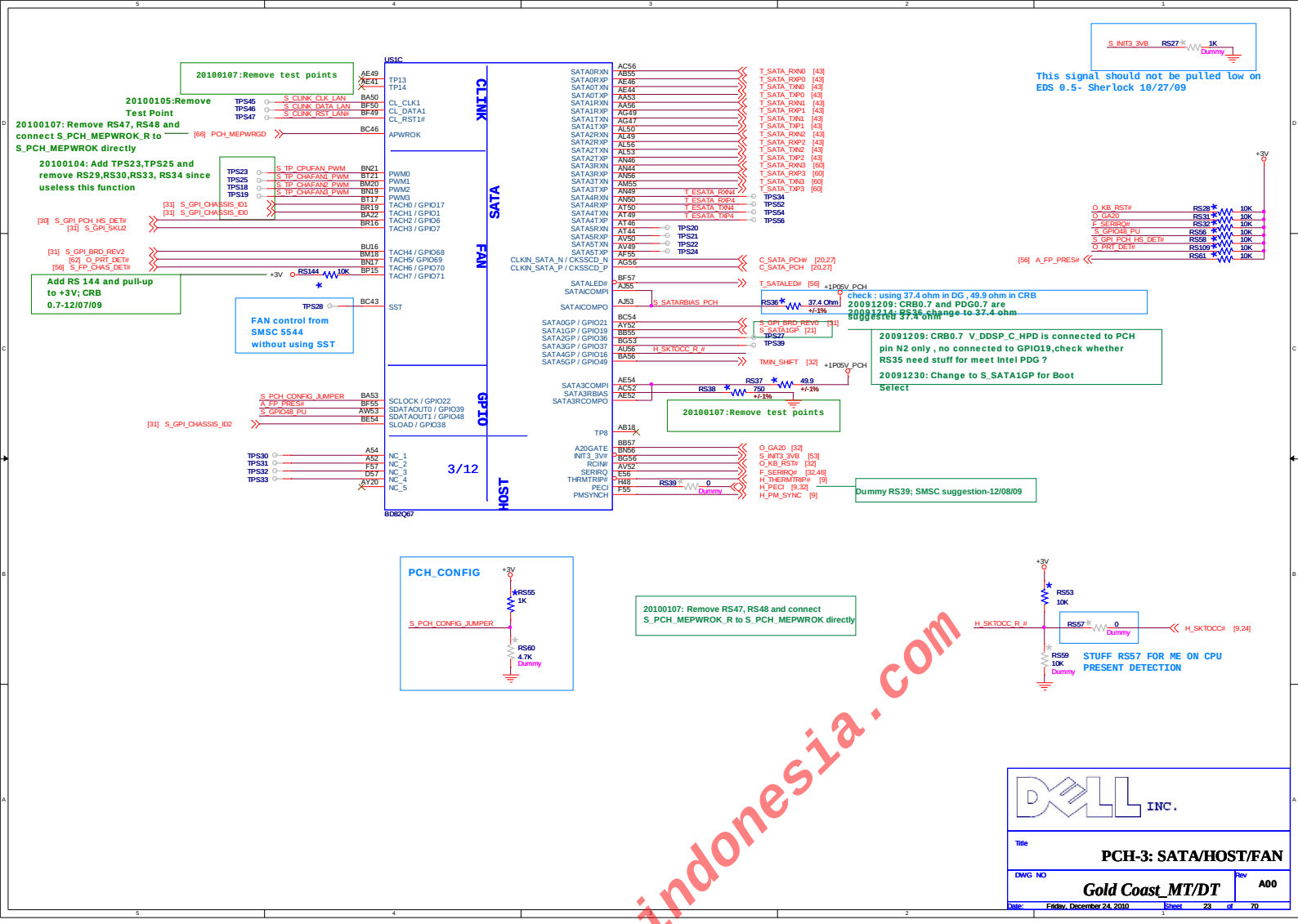
Rev: A00

Date: Friday, December 24, 2010 Sheet 21 of 70






| | |
|---|---|
| Title | PCH-2: DMI/PCIe/USB |
| DWG NO | Gold Coast_MT/DT |
| Rev | A00 |
| Date: | Friday, December 24, 2010 |
| Sheet | 22 of 70 |





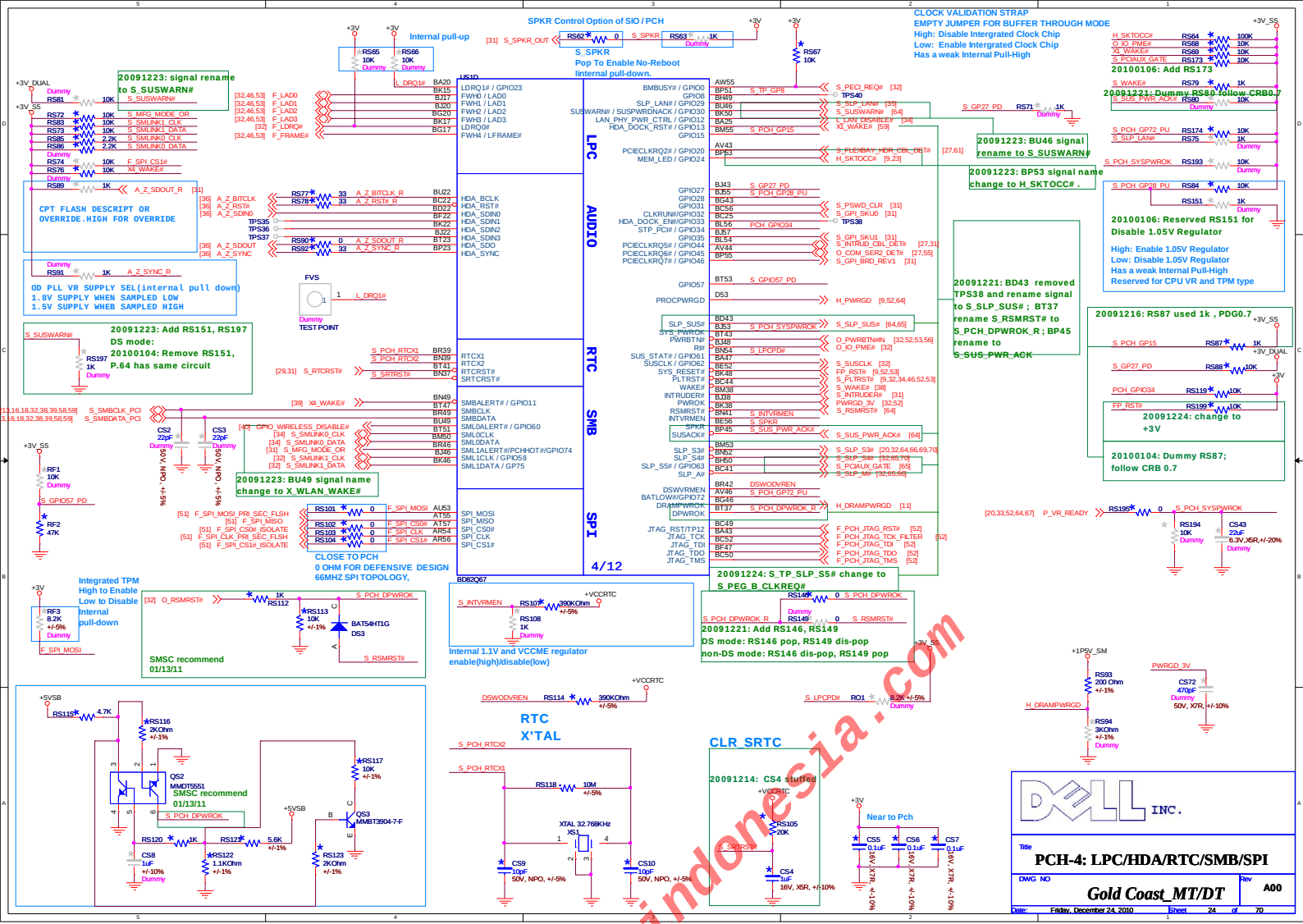

DELL INC.

Title: PCH-3: SATA/HOST/FAN

DWG NO: Gold Coast_MT/DT

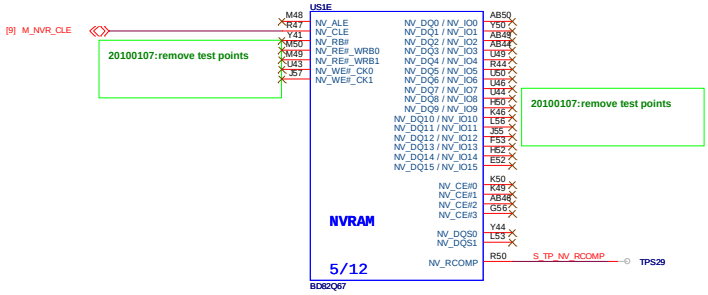
Rev: A00

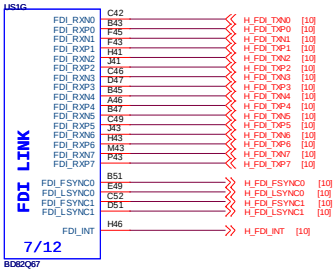
Date: Friday, December 24, 2010 Sheet 23 of 70



20100106: Remove ONFI function since not support

S_NVR_CLE internal pull-down.






DELL INC.

Title: PCH-5/7: NVRAM/FDI

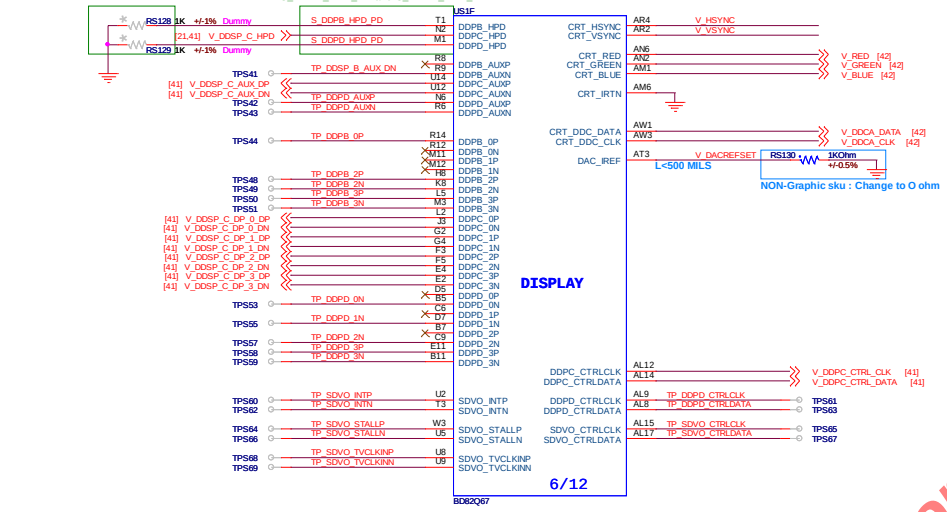
DWG NO: Gold Coast_MT/DT

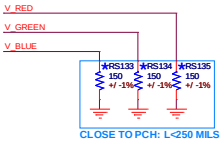
Rev: A00

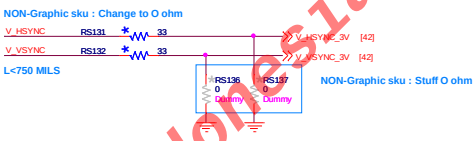
Date: Friday, December 24, 2010 Sheet 25 of 70

20100108: Dummy RS128,RS129: CRB 0.7

20100107: Correct pin T1 and M1 net name to S_DDPB_HPD_PD and S_DDPD_HPD_PD





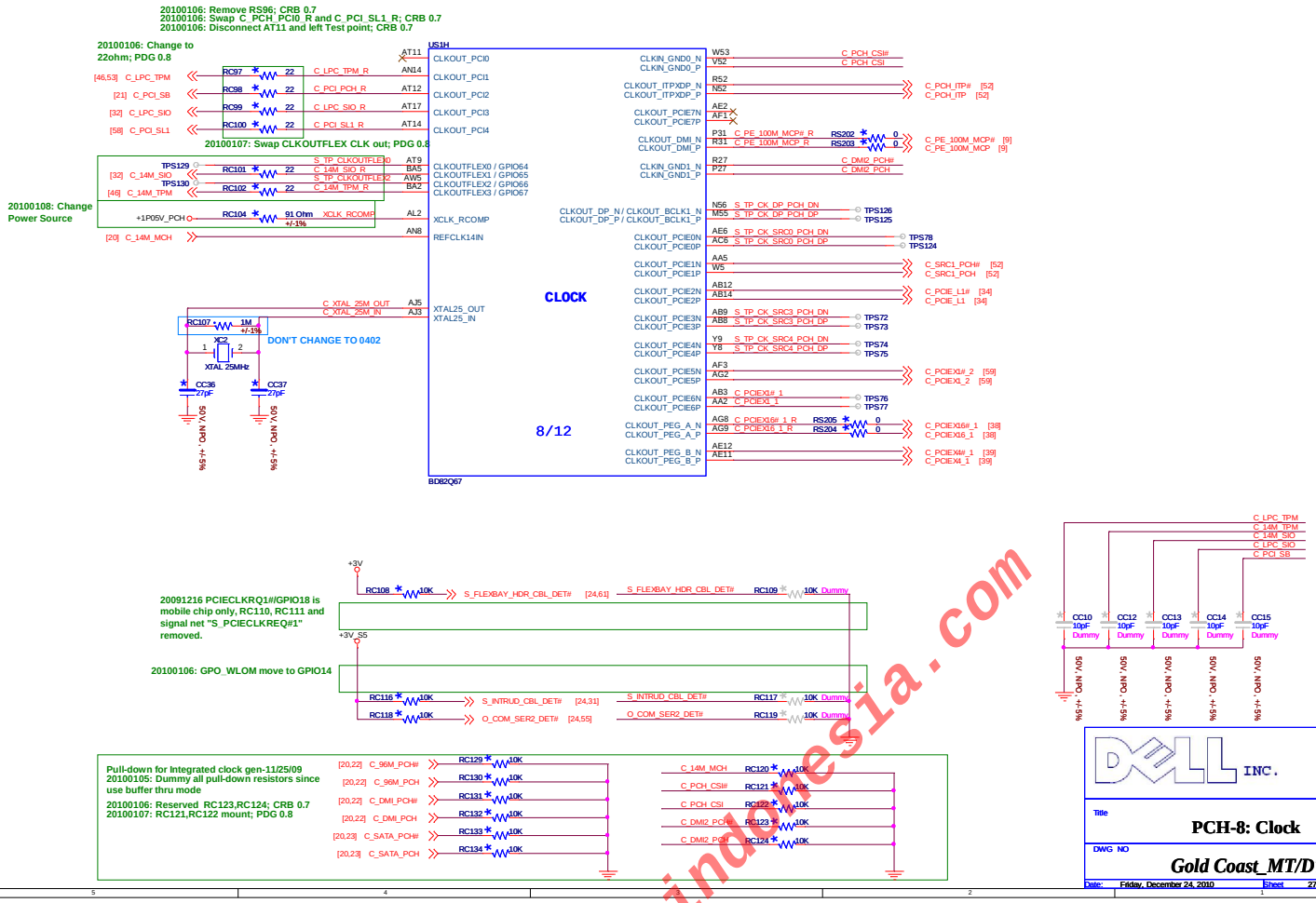

DELL INC.

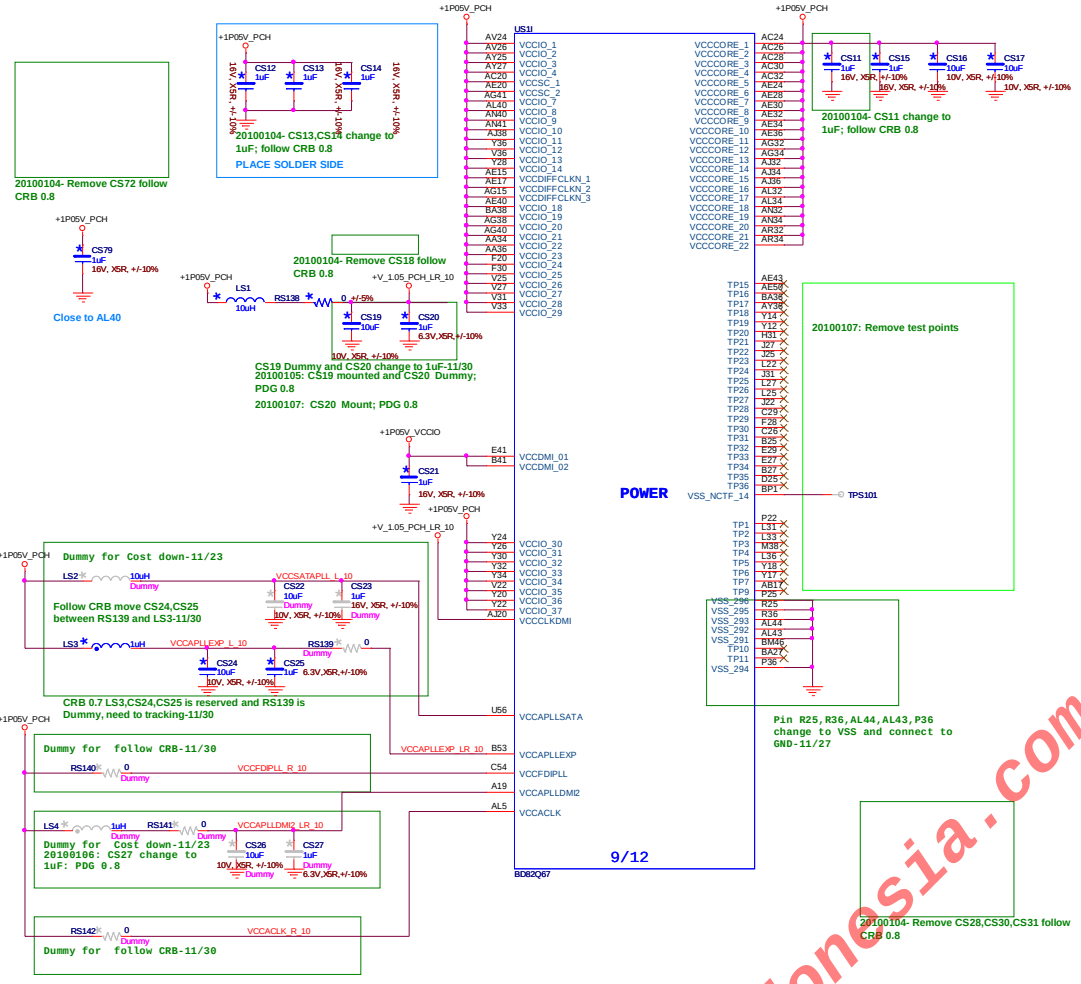
Title: PCH-6: Display

DWG NO: Gold Coast_MT/DT

Rev: A00

Date: Friday, December 24, 2010 Sheet 26 of 70







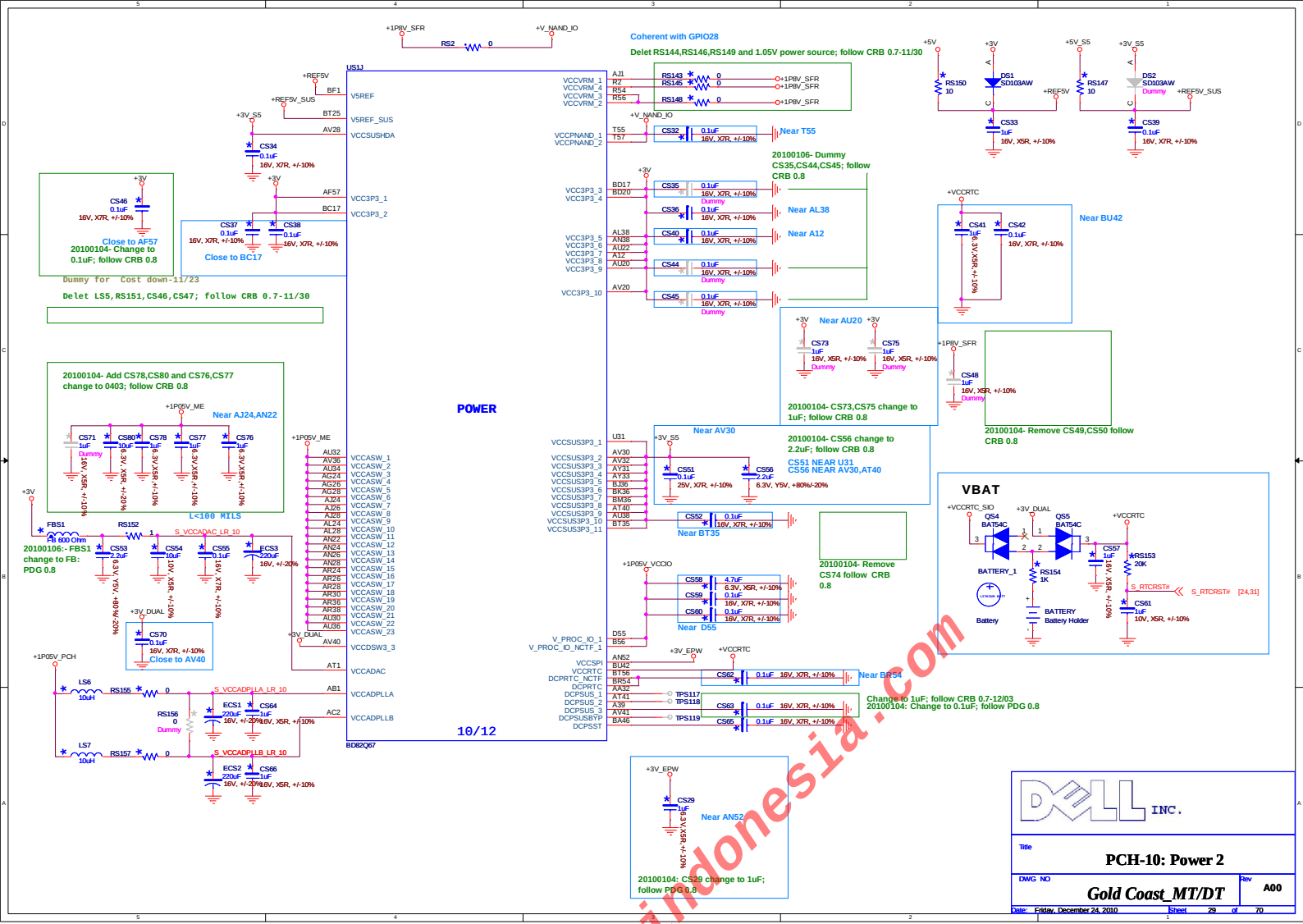

DELL INC.

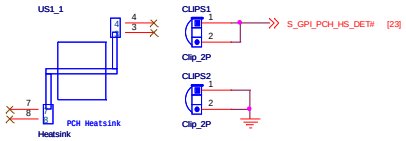
Title: PCH-9: Power 1

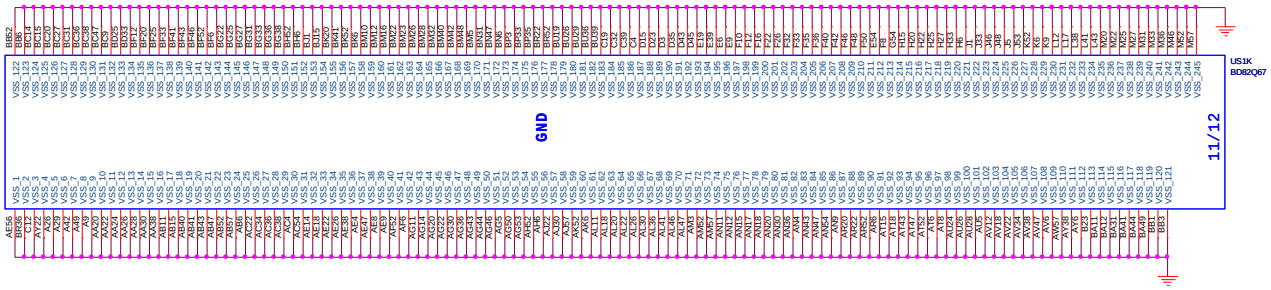
DWG NO: Gold Coast_MT/DT

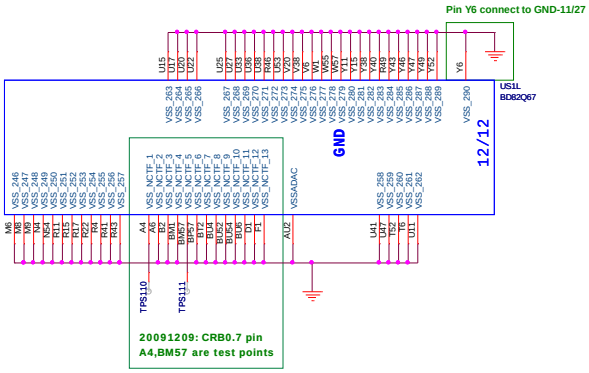
Rev: A00

Date: Friday, December 24, 2010 Sheet 28 of 70








DELL INC.

Title

**PCH-11: GND**

DWG NO

*Gold Coast_MT/DT*

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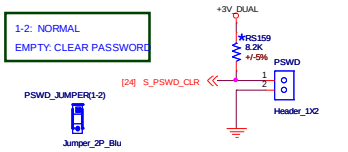
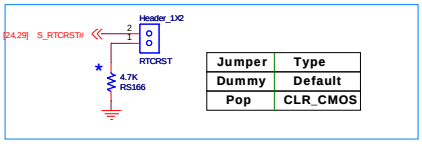
## Clear Password





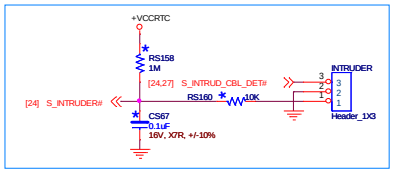


## CLR_CMOS

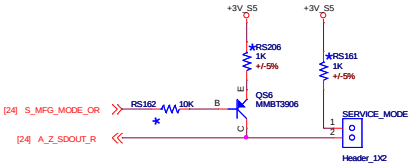



| Jumper | Type |
|---|---|
| Dummy | Default |
| Pop | CLR_CMOS |

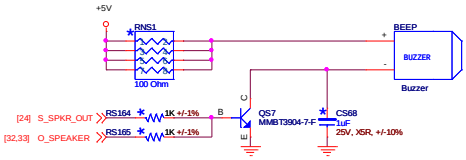
## Chassis Intruder



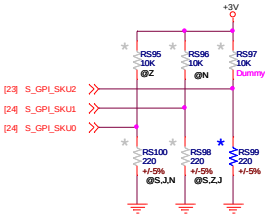

## SERVICE_MODE




## BEEP




## SKU ID



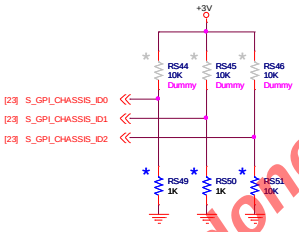

### SKU ID

| SKU1 | SKU0 | Type |
|---|---|---|
| 0 | 0 | TPM |
| 0 | 1 | TCM |
| 1 | 0 | non TPM/TCM |
| 1 | 1 | Reserved |

## Chassis ID

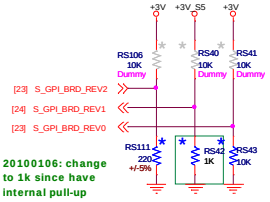
**check : need to update table**

| ID2 | ID1 | ID0 | Type |
|---|---|---|---|
| 1 | 0 | 1 | SFF |
| 1 | 0 | 0 | Tambor |
| 0 | 0 | 0 | MT/DT |
| 0 | 1 | 1 | USFF |




## BOARD ID

| Rev2 | Rev1 | Rev0 | Type |
|---|---|---|---|
| 0 | 0 | 0 | Default |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |




20100106: change to 1k since have internal pull-up 10k

DELL INC.

Title: **PCH MISC Conn/BUZ/ID**

DWG NO: ***Gold Coast_MT/DT***

Rev: A00

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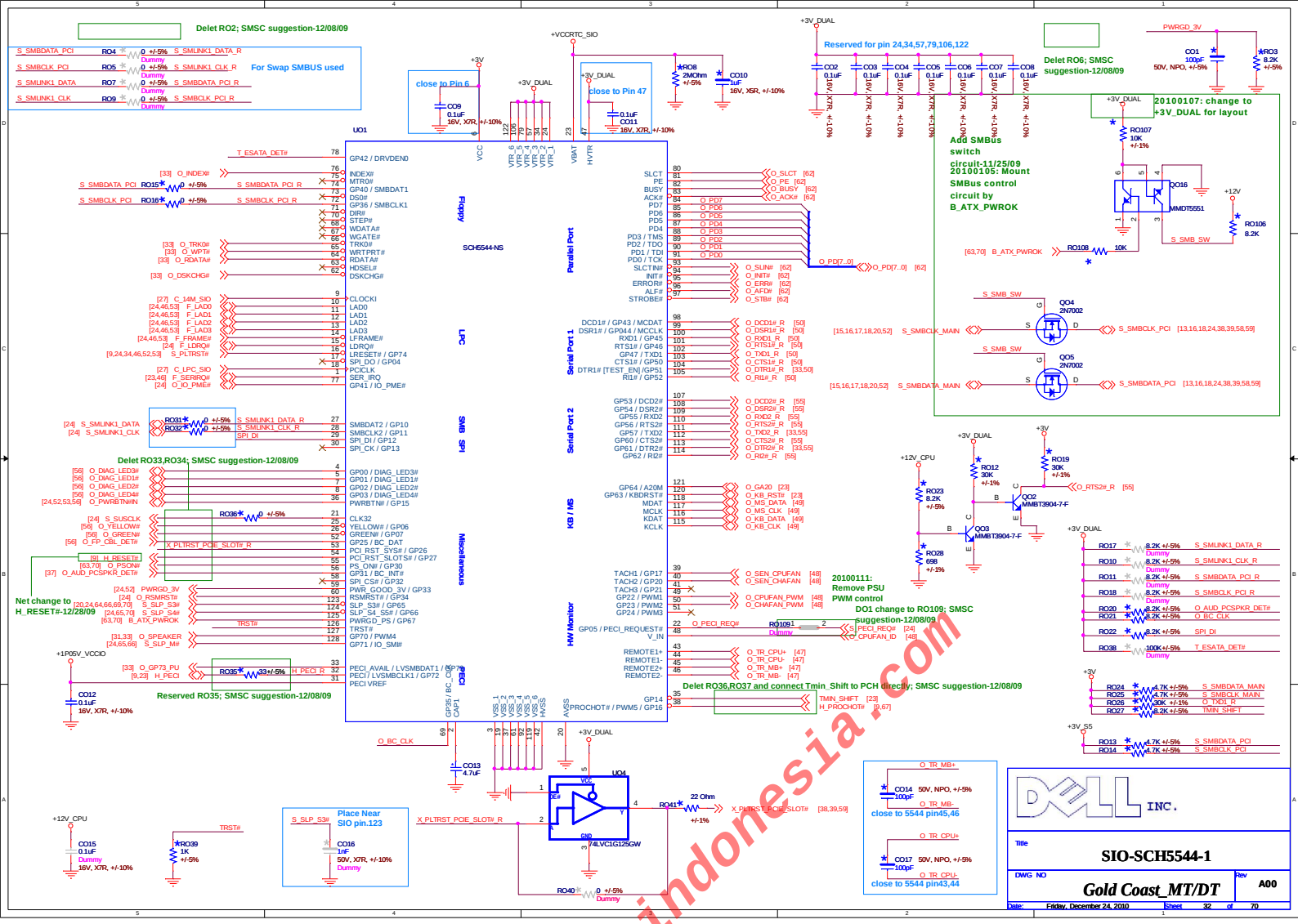

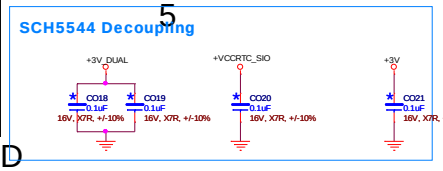


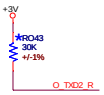


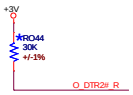


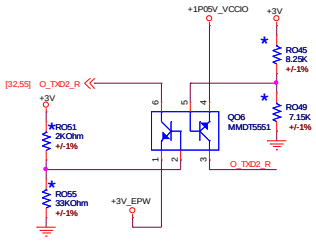


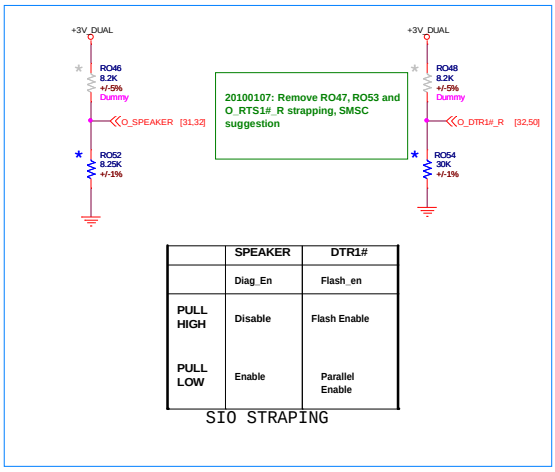


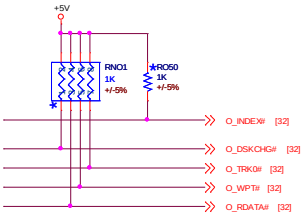


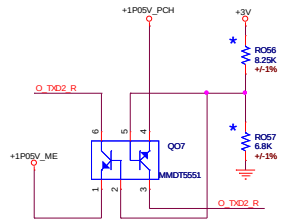


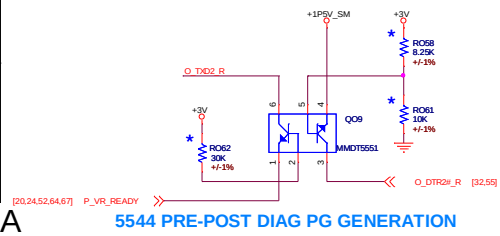


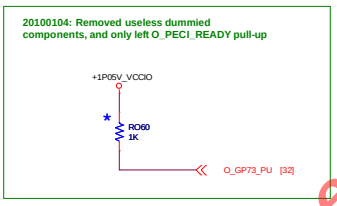


5544 PRE-POST DIAG PG GENERATION

DELL INC.

Title: SIO-SCH5544-2 (MISC)

DWG NO: Gold Coast_MT/DT

Rev: A00

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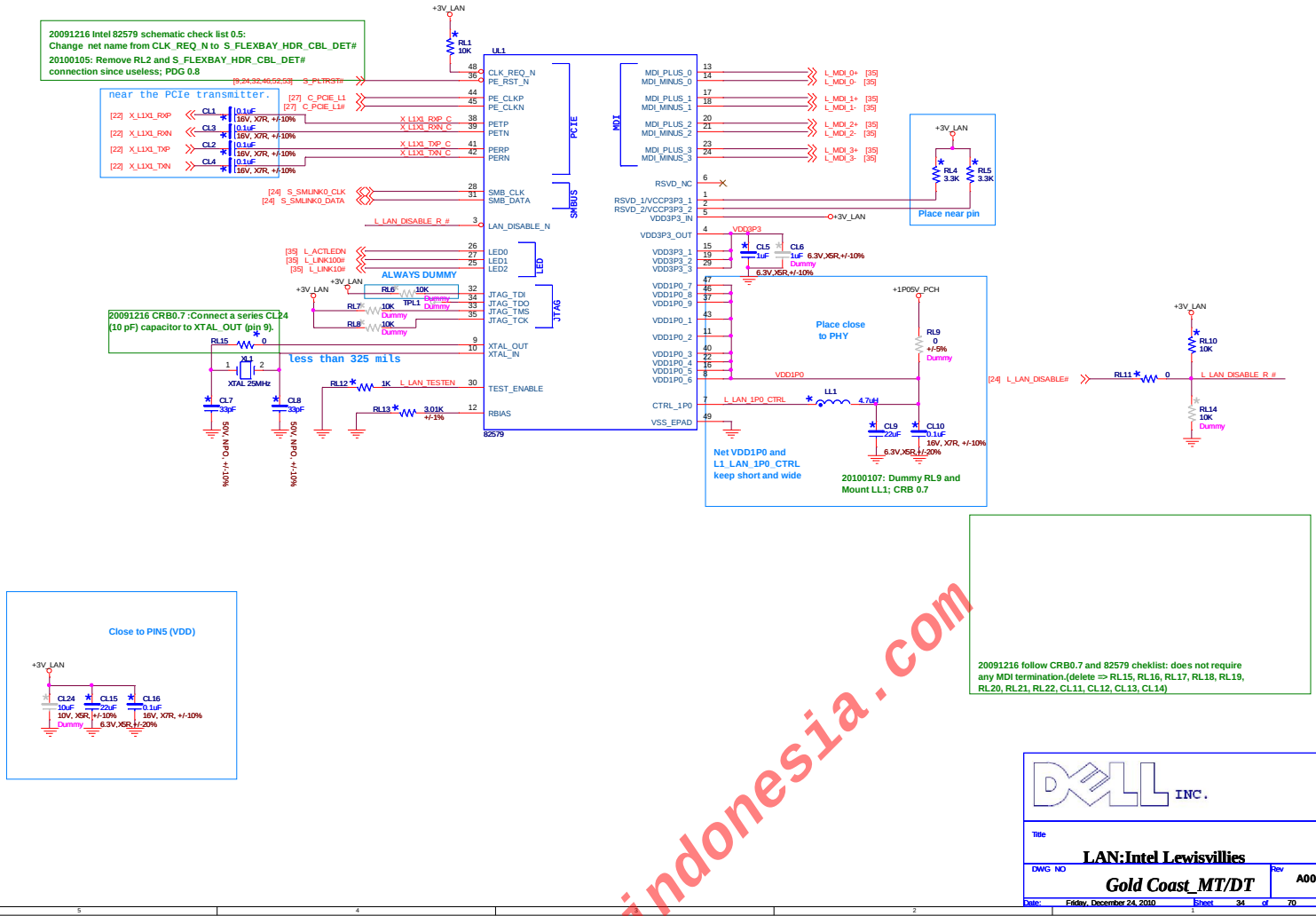




DELL INC.

Title

**LAN:Intel Lewisvillies**

| DWG NO | Rev |
|---|---|
| *Gold Coast_MT/DT* | A00 |

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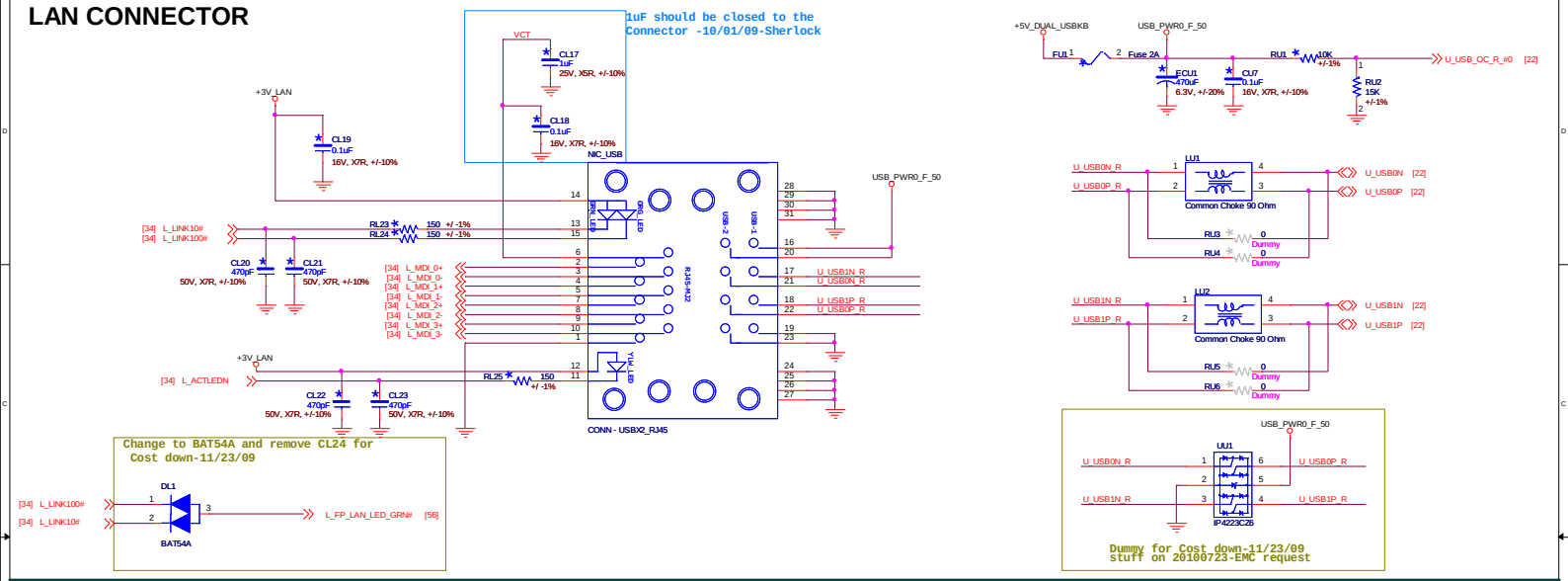
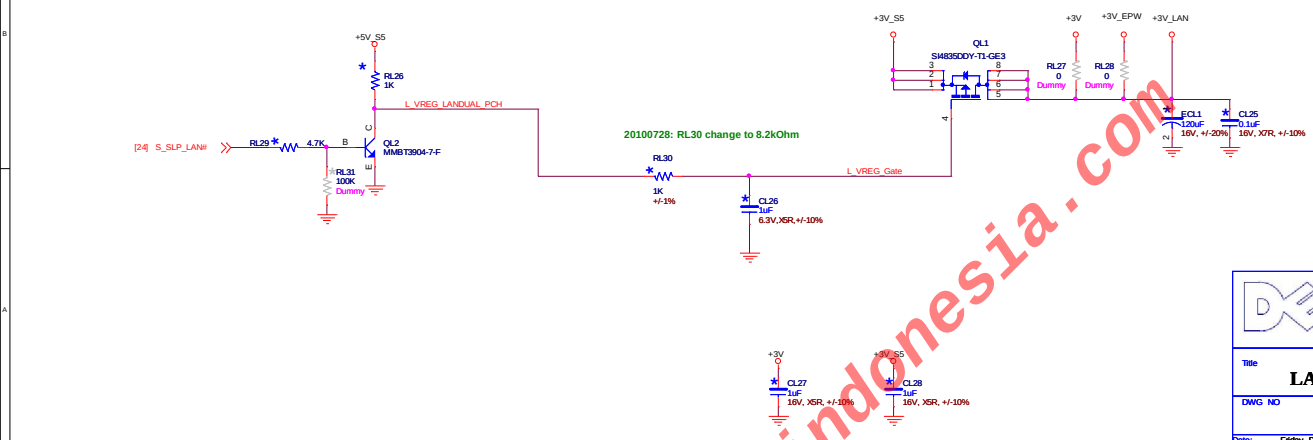
# LAN CONNECTOR




# LAN POWER




DELL INC.

Title: LAN Power & LAN/USB Conn

DWG NO: Gold Coast_MT/DT

Rev: A00

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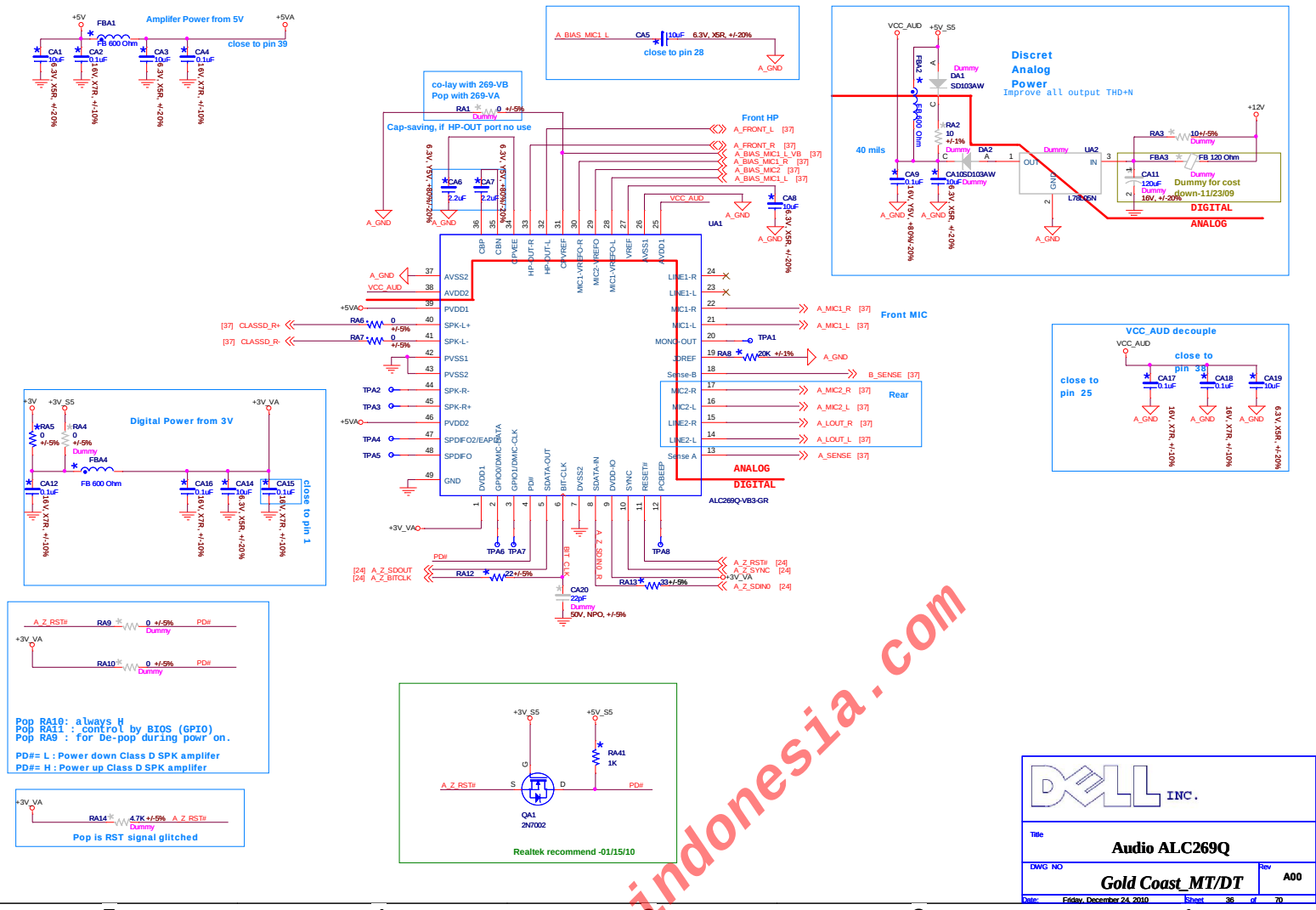




DELL INC.

Title: Audio ALC269Q

DWG NO: Gold Coast_MT/DT

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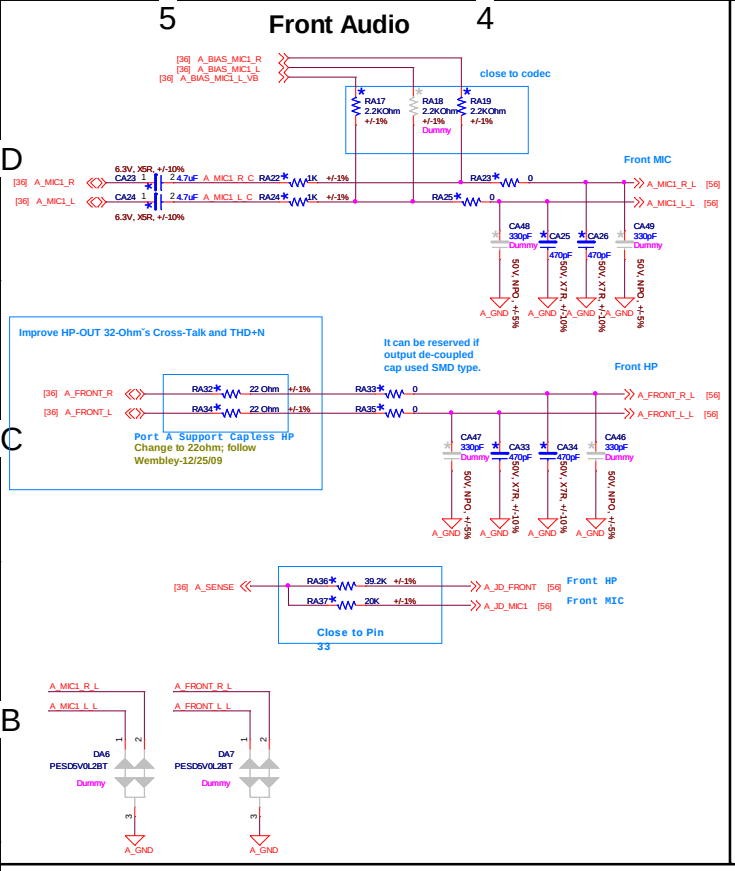


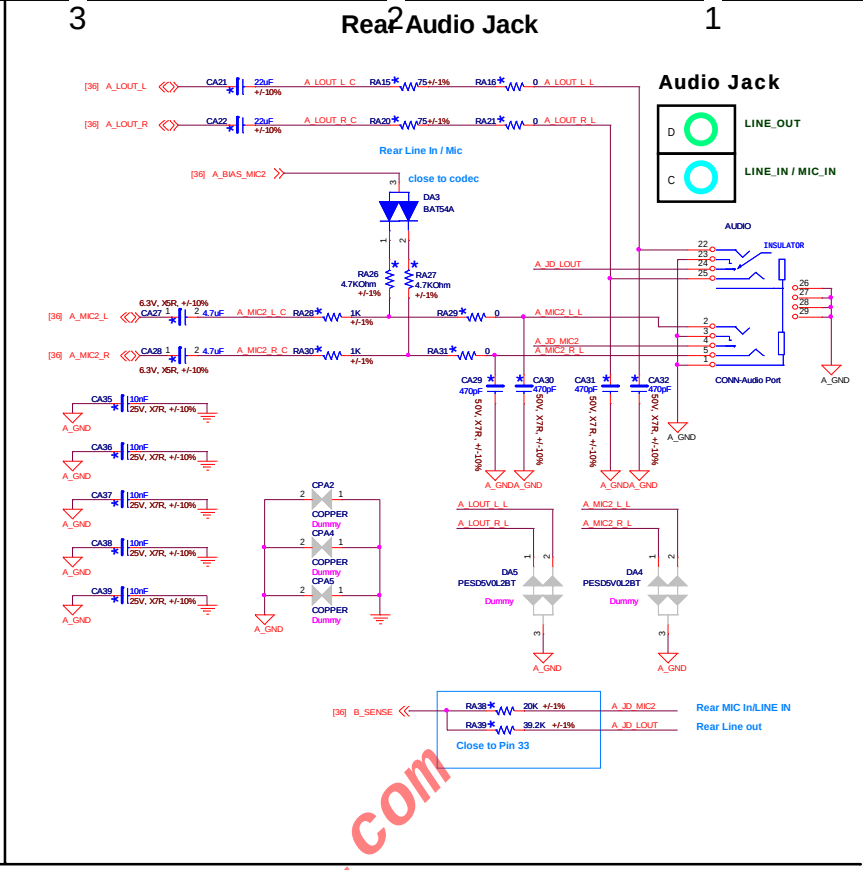


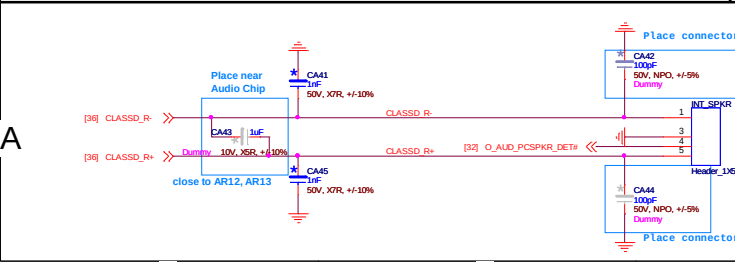


CHASSIS
SPEAKER

DELL INC.

Title: Audio Conn

DWG NO: Gold Coast_MT/DT

Rev: A00

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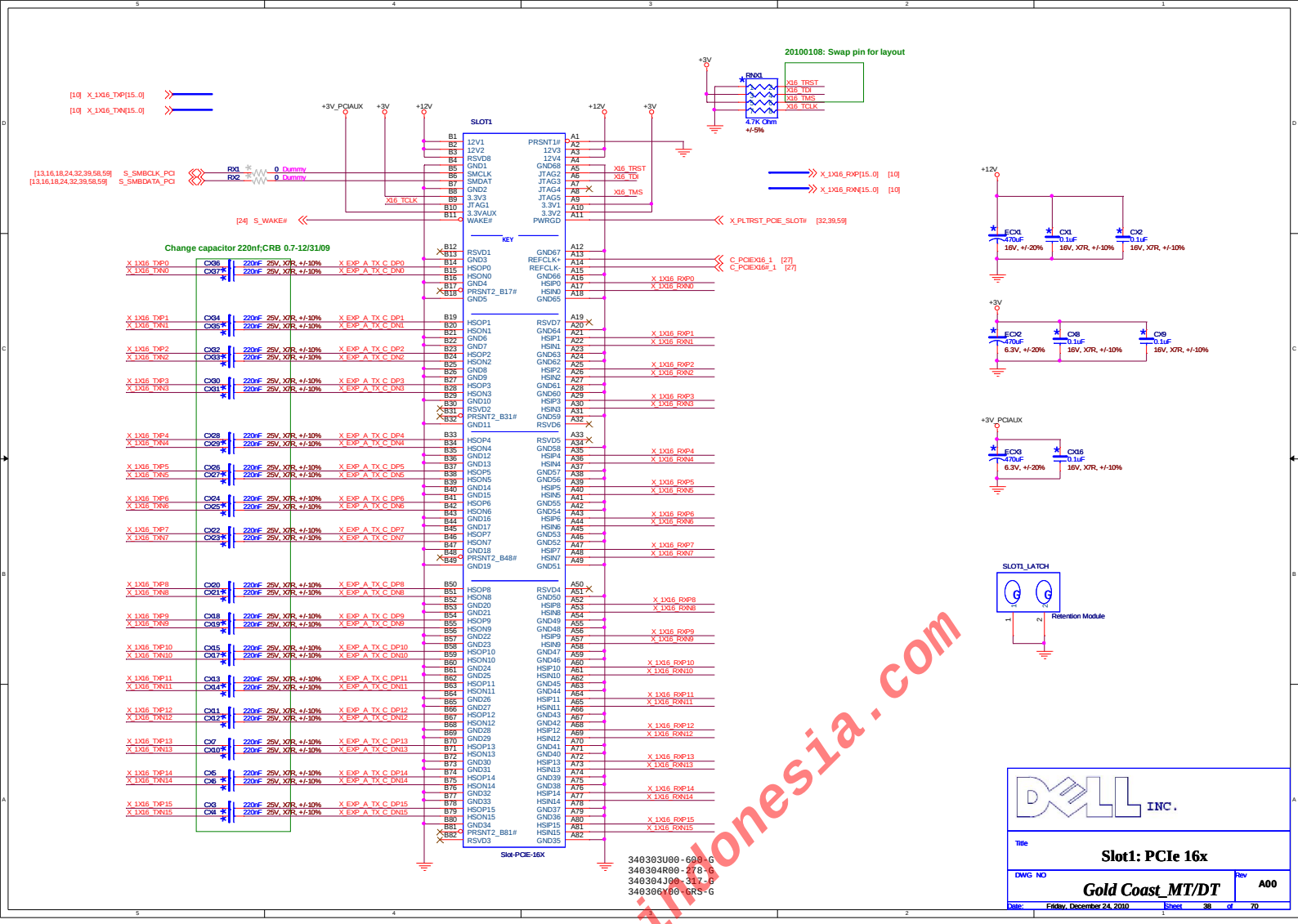
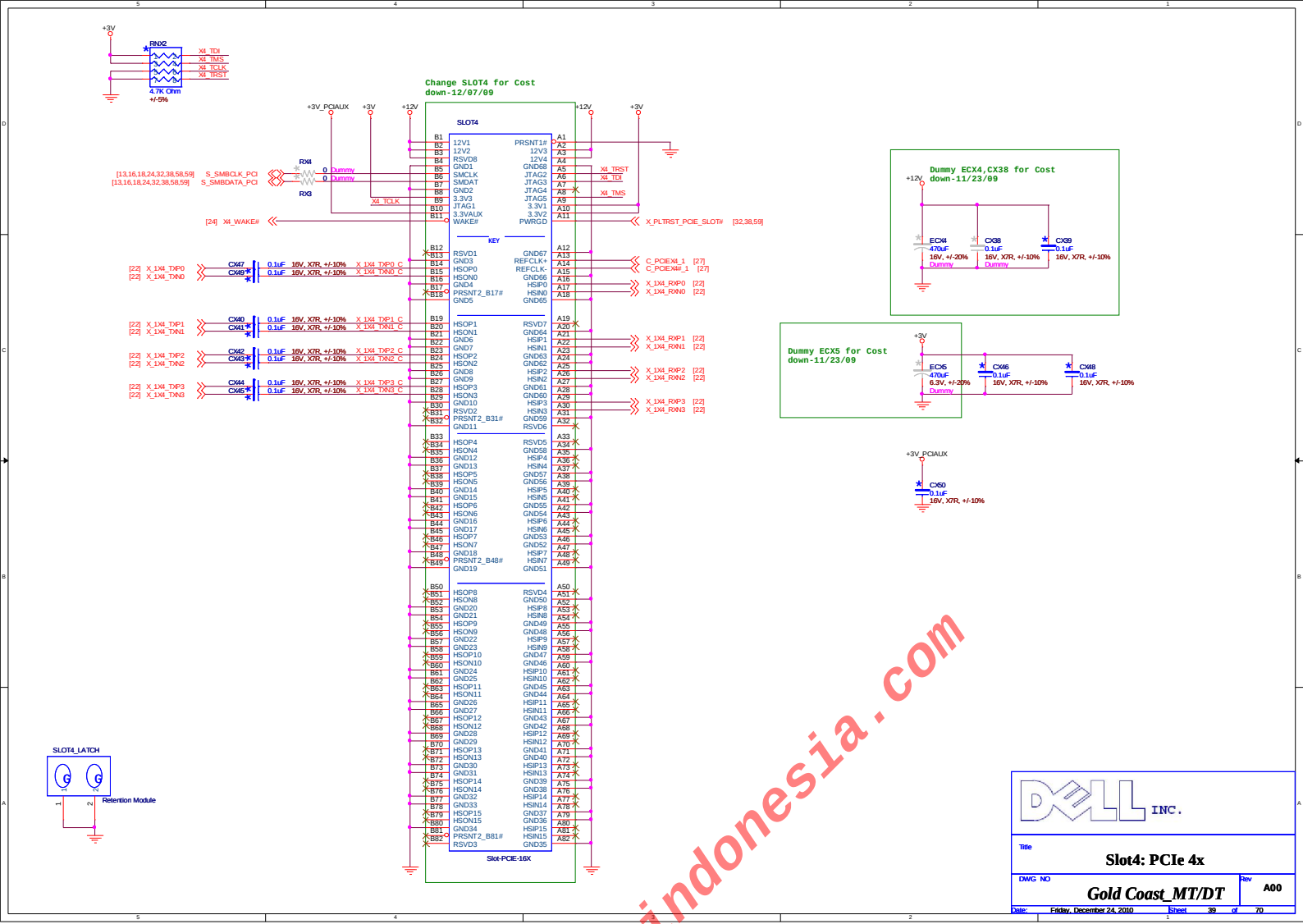






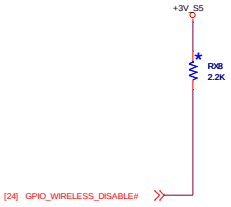

DELL INC.

Title: Slot4: PCIe 4x

DWG NO: Gold Coast_MT/DT

Rev: A00

Date: Friday, December 24, 2010 Sheet 39 of 70




DELL INC.

Title

**TBD**

DWG NO

***Gold Coast_MT/DT***

Rev

A00

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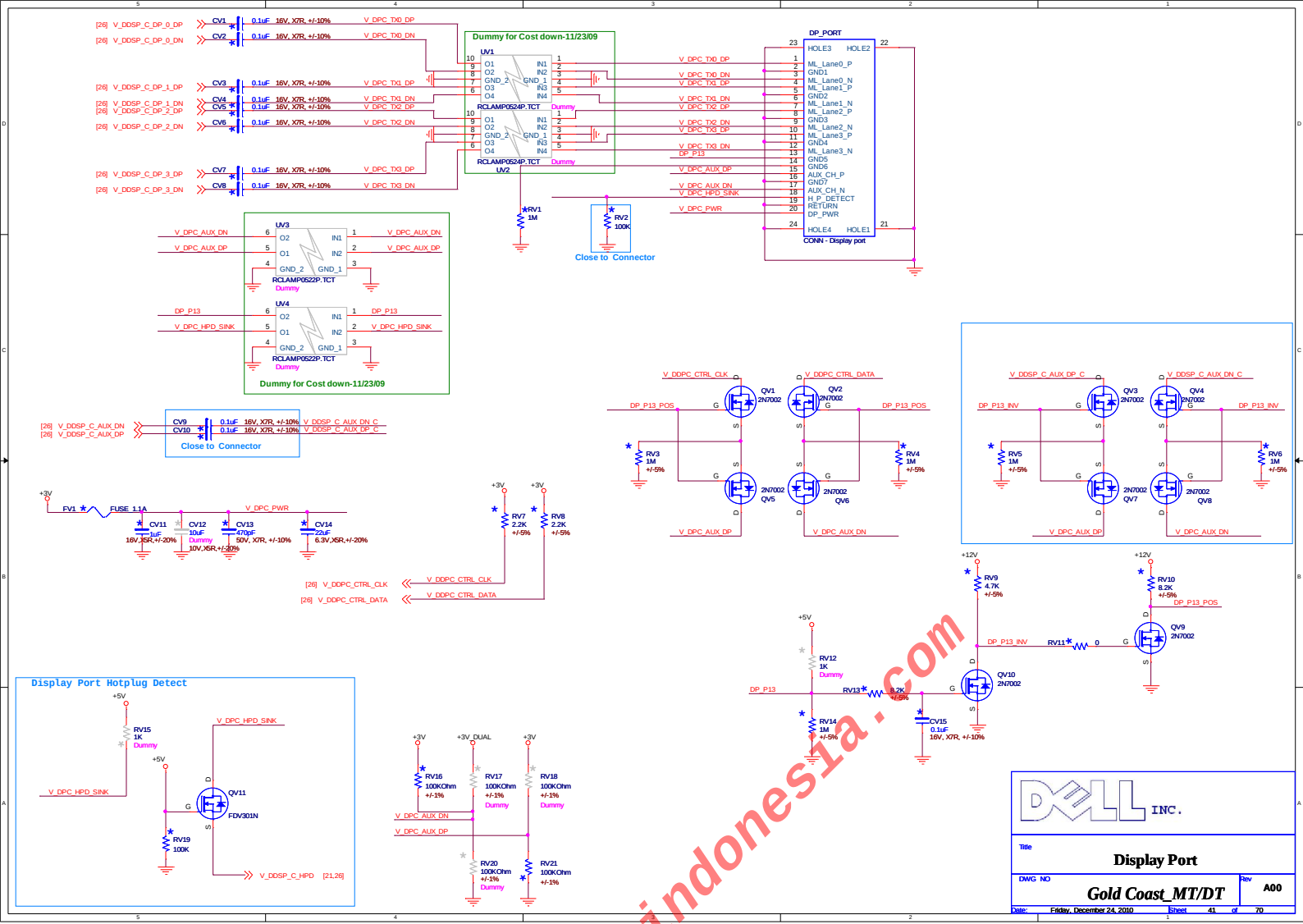
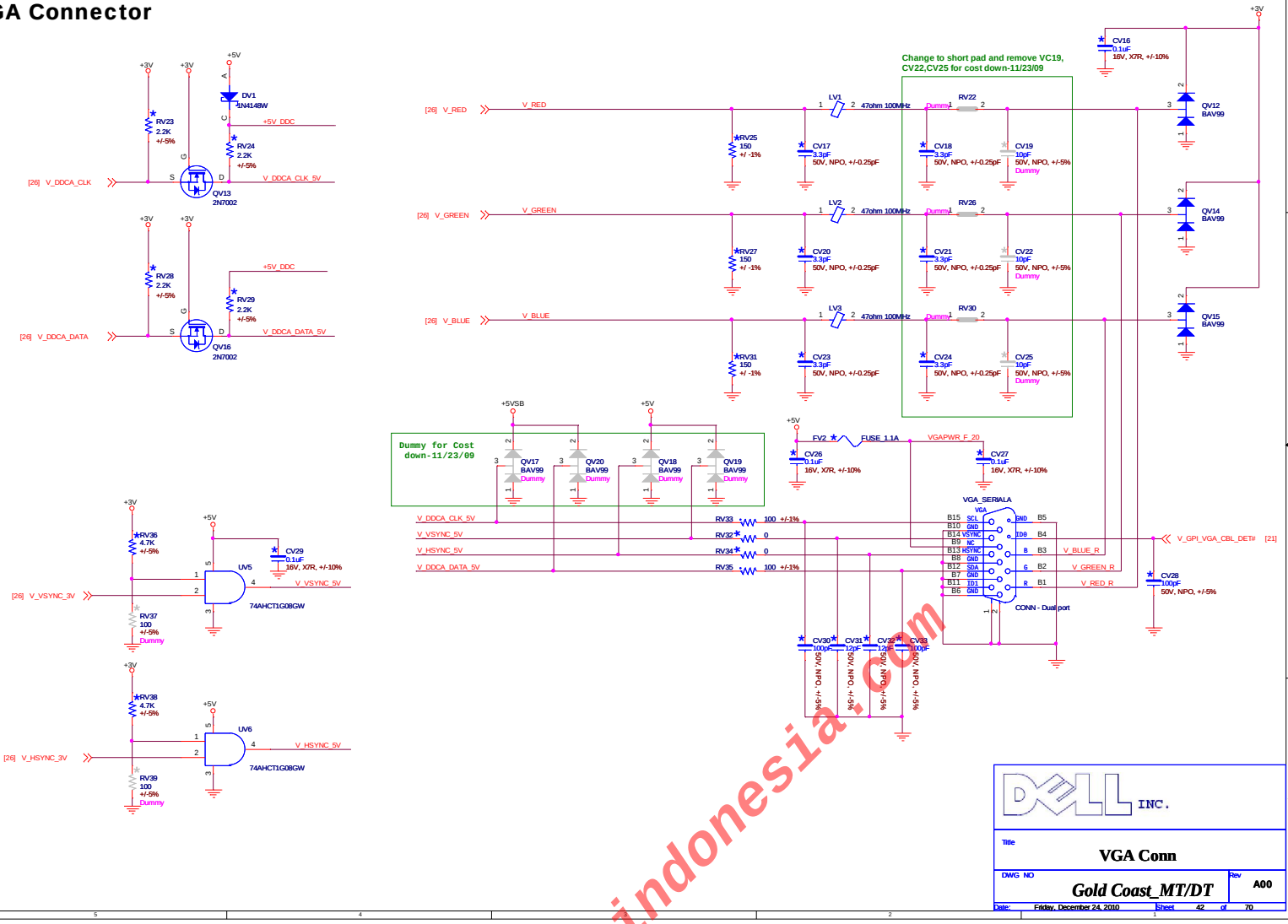


# VGA Connector




DELL INC.

Title: VGA Conn

DWG NO: Gold Coast_MT/DT

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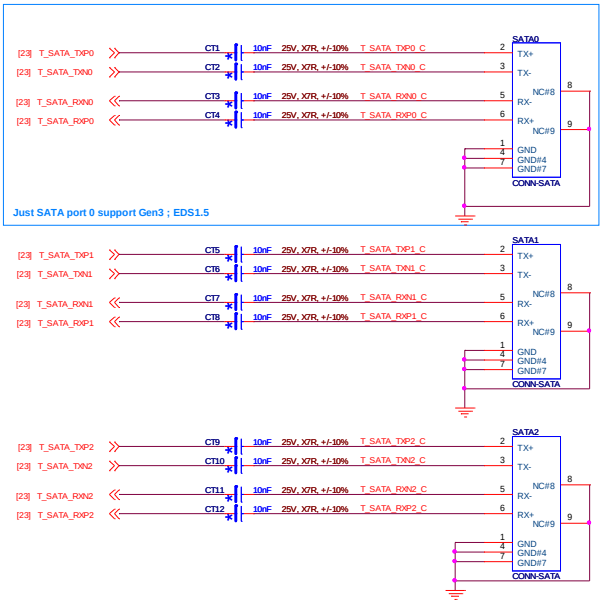
# SATA x 3






DELL INC.

Title: **SATA Conn**

DWG NO: ***Gold Coast_MT/DT***

Rev: A00

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DELL INC.

Title

**TBD**

DWG NO

***Gold Coast_MT/DT***

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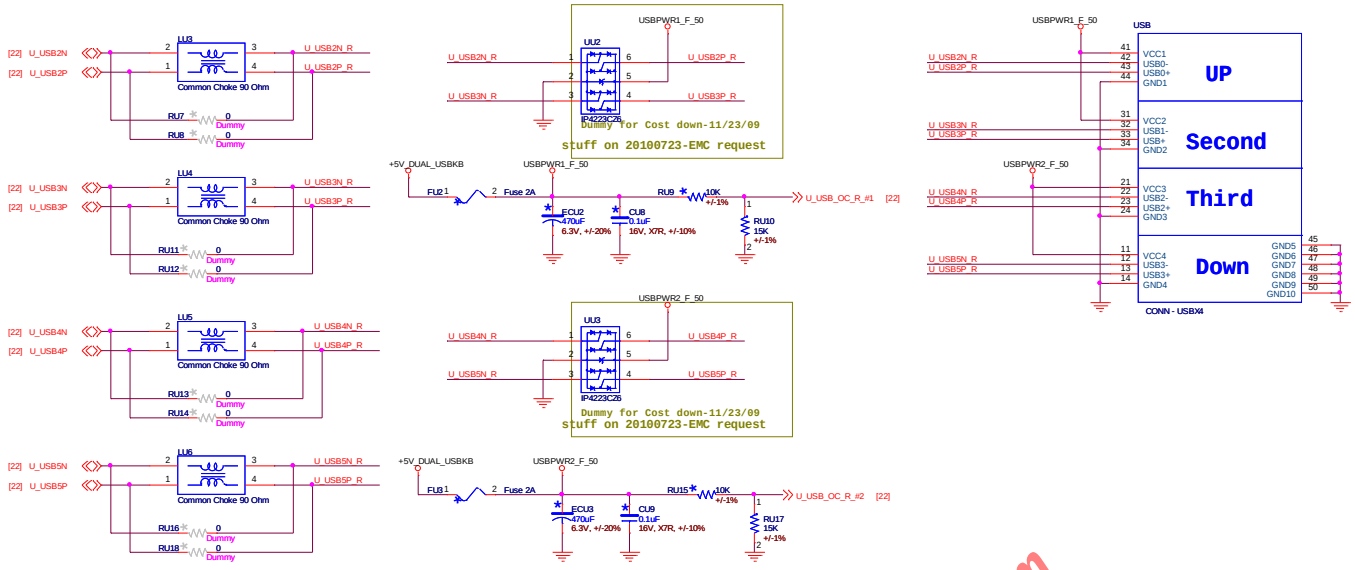
# Rear USB CONNECTOR






DELL INC.

Title: **Rear USB**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

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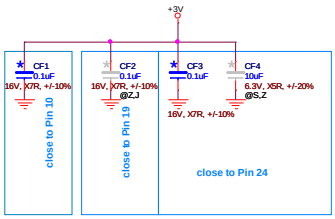
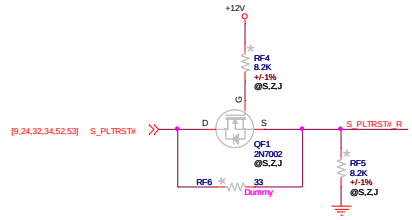
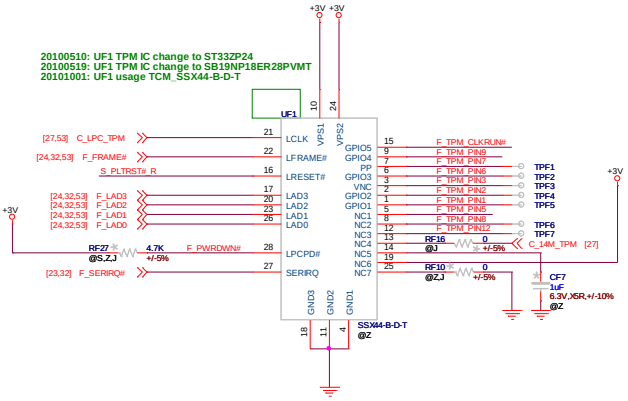
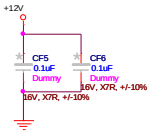
# TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

| | | |
|---|---|---|
| (Default) ST Micro | POP S | CF4 |
| ZTE | POP Z | CF2,CF4,CF7,RF10,RF19,RF20,RF21 |
| Jetway | POP J | CF2,CF8,RF10,RF16,RF21 |

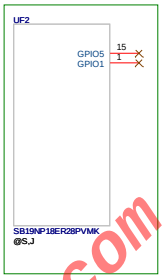



20101001: add UF2 usage TPM_SB19NP18ER28PVMK





DELL INC.

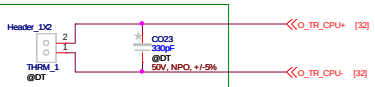
Title: TPM & TCM

DWG NO: Gold Coast_MT/DT

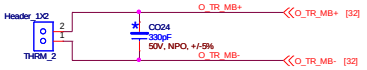
Rev: A00

Date: Friday, December 24, 2010 Sheet 46 of 70

Change net to O_TR_MB+/-; SMSC suggestion-12/08/09
Removed THRM1 since useless-01/01/10




Dummy THRM2,CO23; ME suggestion-12/04/09




THERMAL SENSOR



DELL INC.

Title: Thermal Sensor Conn

DWG NO: Gold Coast_MT/DT

Rev: A00

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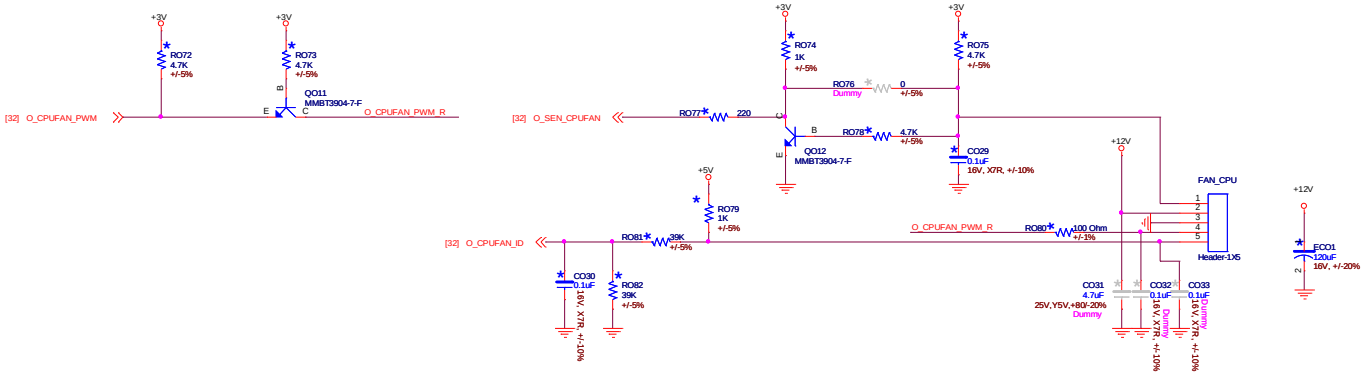
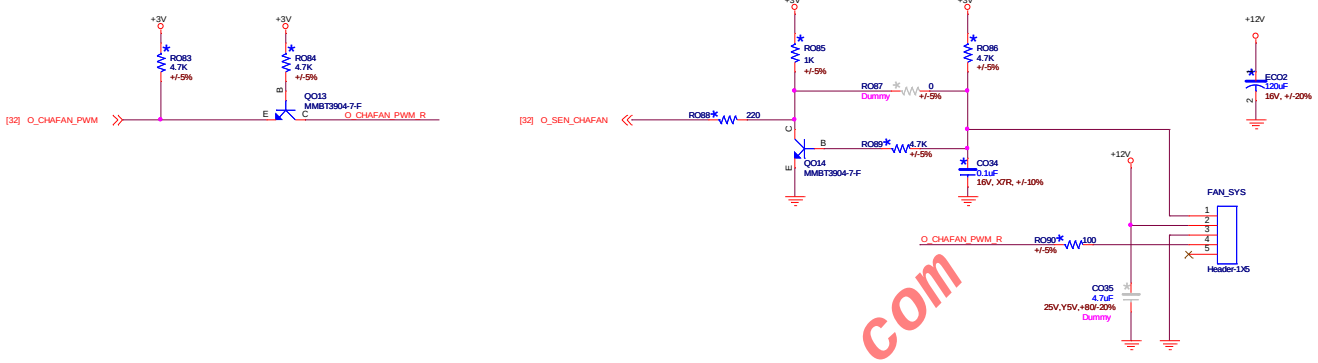
## CPU Fan




## SYS Fan




## PSU Fan

20100111: Remove PSU PWM control

| | |
|---|---|
| Title | FAN |
| DWG NO | Gold Coast_MT/DT |
| Rev | A00 |
| Date: | Friday, December 24, 2010 |
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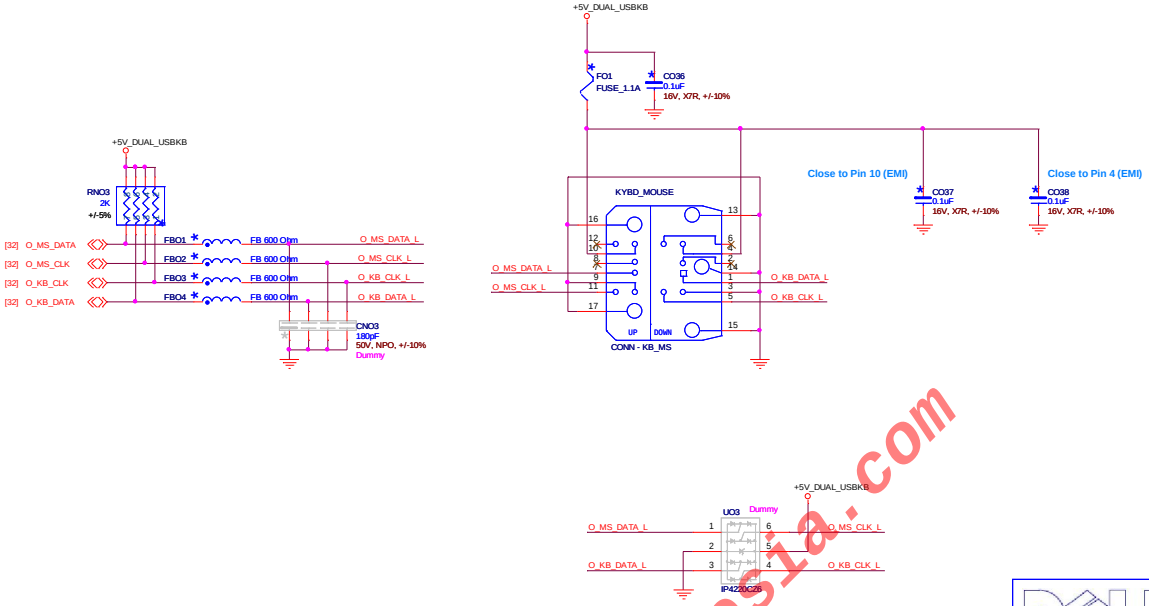
# KB/MS






DELL INC.

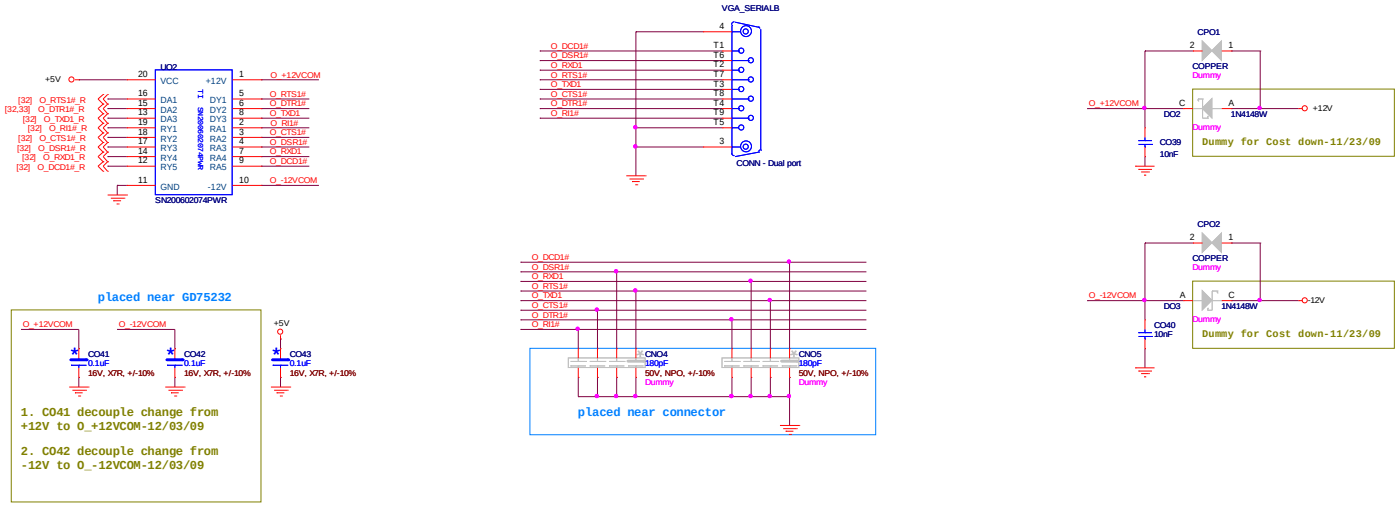
Title: **PS2 Conn**

DWG NO: ***Gold Coast_MT/DT***

Rev: A00

Date: Friday, December 24, 2010 Sheet 49 of 70

# Serial Port 1






DELL INC.

Title: COM1

DWG NO: Gold Coast_MT/DT

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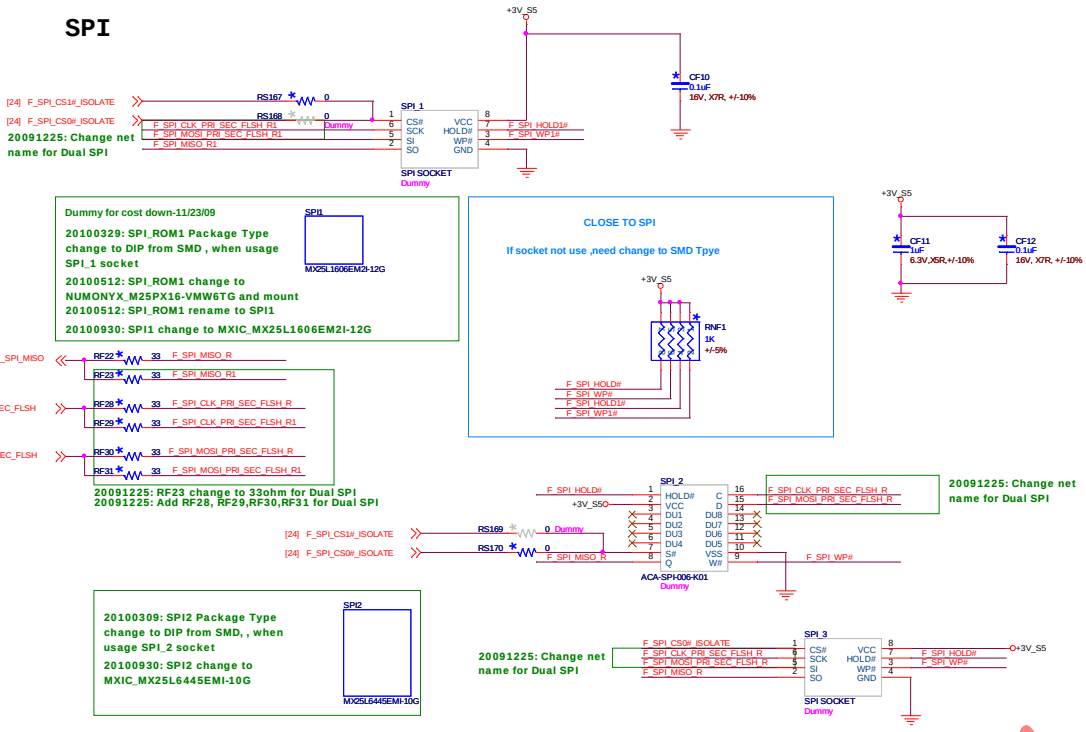
# SPI






DELL INC.

Title: SPI

DWG NO: Gold Coast_MT/DT

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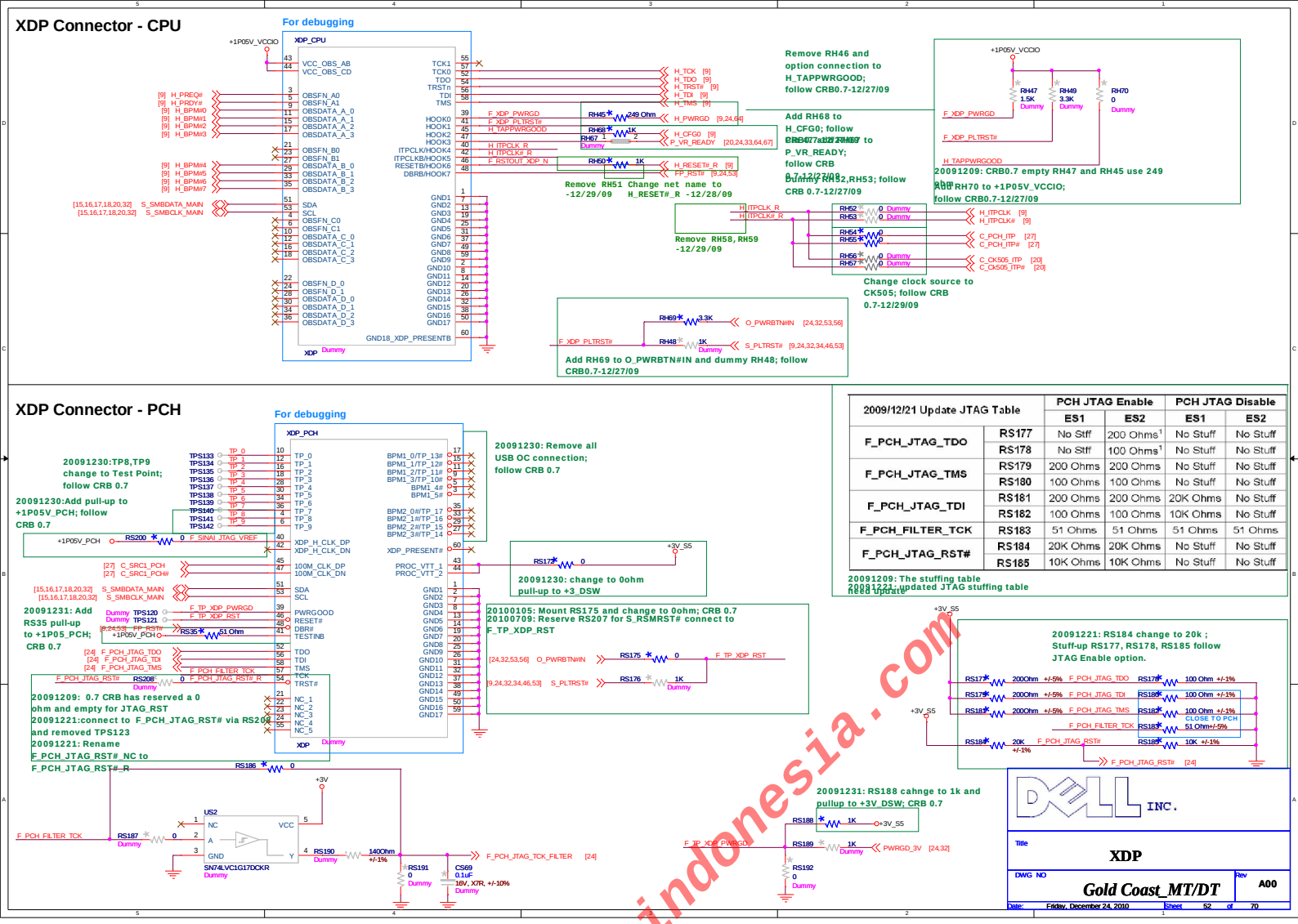
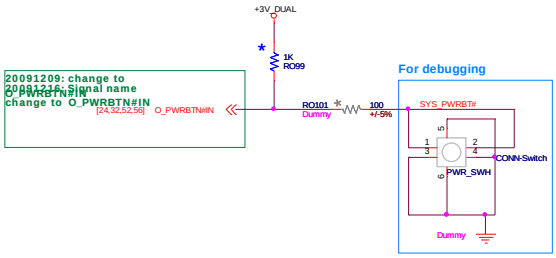


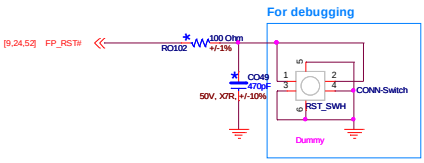

| 2009/12/21 Update JTAG Table | | PCH JTAG Enable | | PCH JTAG Disable | |
|---|---|---|---|---|---|
| | | ES1 | ES2 | ES1 | ES2 |
| F_PCH_JTAG_TDO | RS177 | No Stff | 200 Ohms[1] | No Stuff | No Stuff |
| | RS178 | No Stff | 100 Ohms[1] | No Stuff | No Stuff |
| F_PCH_JTAG_TMS | RS179 | 200 Ohms | 200 Ohms | No Stuff | No Stuff |
| | RS180 | 100 Ohms | 100 Ohms | No Stuff | No Stuff |
| F_PCH_JTAG_TDI | RS181 | 200 Ohms | 200 Ohms | 20K Ohms | No Stuff |
| | RS182 | 100 Ohms | 100 Ohms | 10K Ohms | No Stuff |
| F_PCH_FILTER_TCK | RS183 | 51 Ohms | 51 Ohms | 51 Ohms | 51 Ohms |
| F_PCH_JTAG_RST# | RS184 | 20K Ohms | 20K Ohms | No Stuff | No Stuff |
| | RS185 | 10K Ohms | 10K Ohms | No Stuff | No Stuff |

20091209: The stuffing table
20091221: updated JTAG stuffing table need update

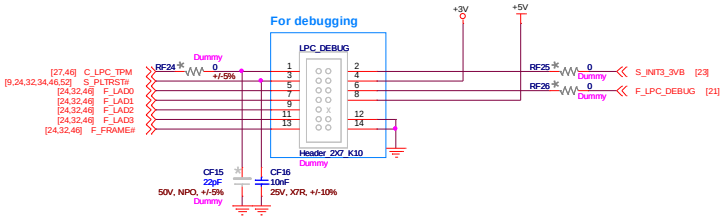
## Power Bottom

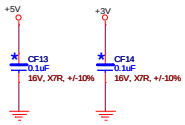



## Reset Bottom




# LPC DEBUG






DELL INC.

Title: **Pilot Run Conn**

DWG NO: ***Gold Coast_MT/DT***

Rev: A00

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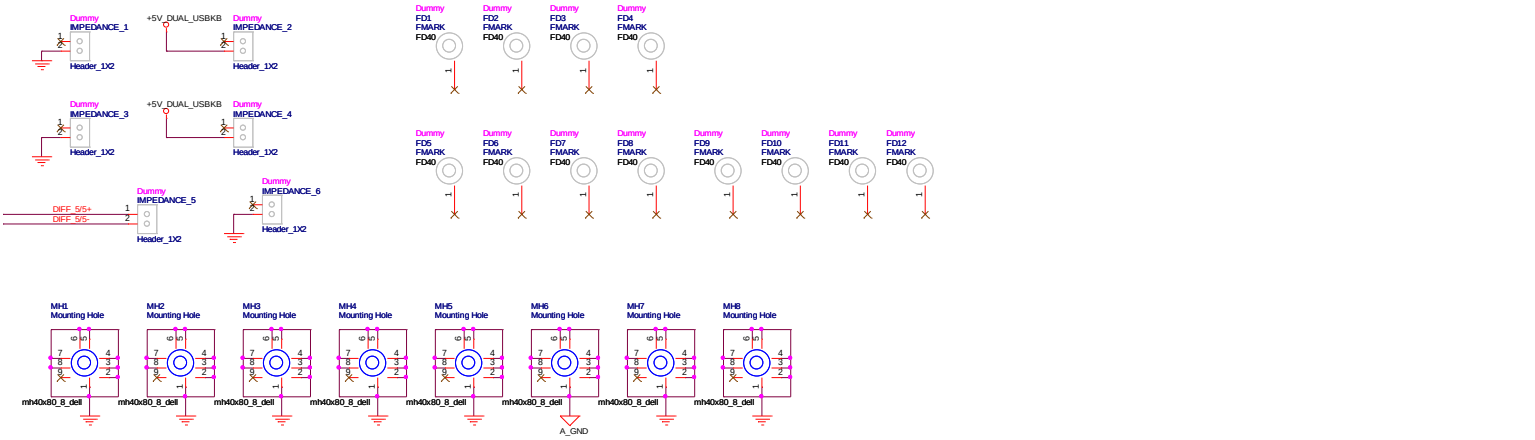
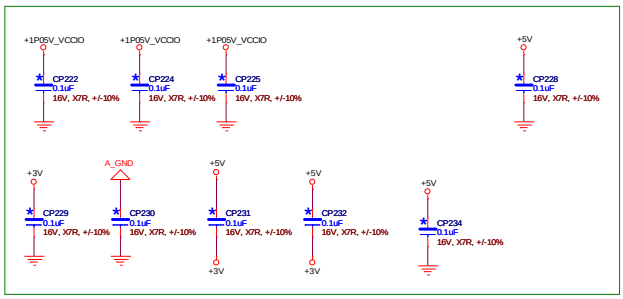
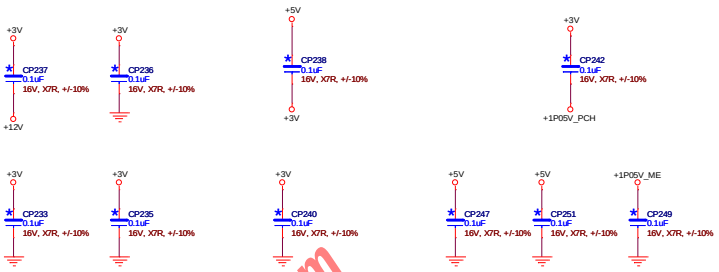


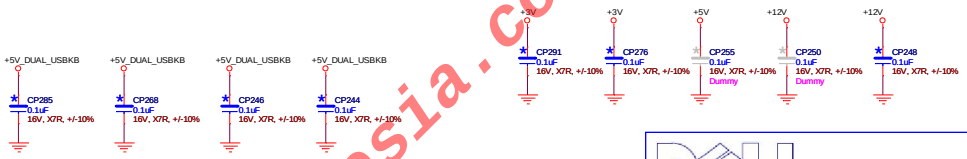




20100108: Add for EMI




DELL INC.

Title: **EMI**

DWG NO: ***Gold Coast_MT/DT***

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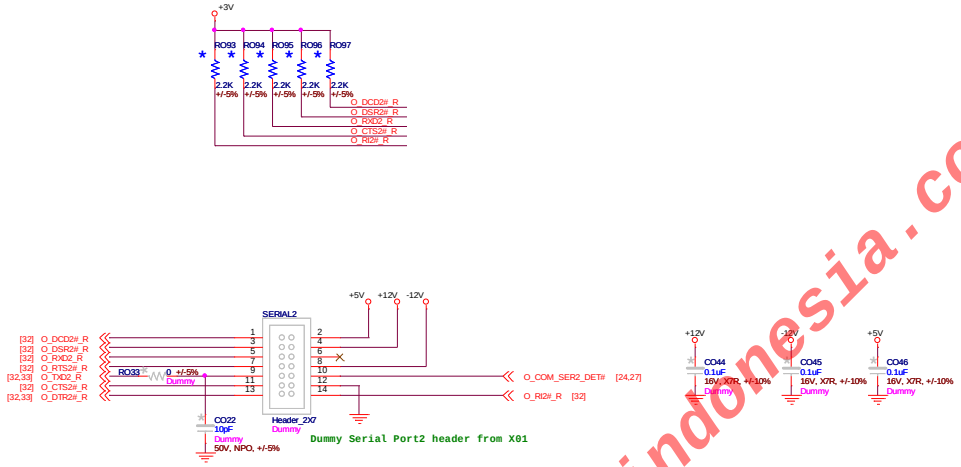
Move PWR_SW conn to
page56 20091126

## Serial Port 2 Header




DELL INC.

Title
**COM2 HDR**

DWG NO
***Gold Coast_MT/DT***

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A00

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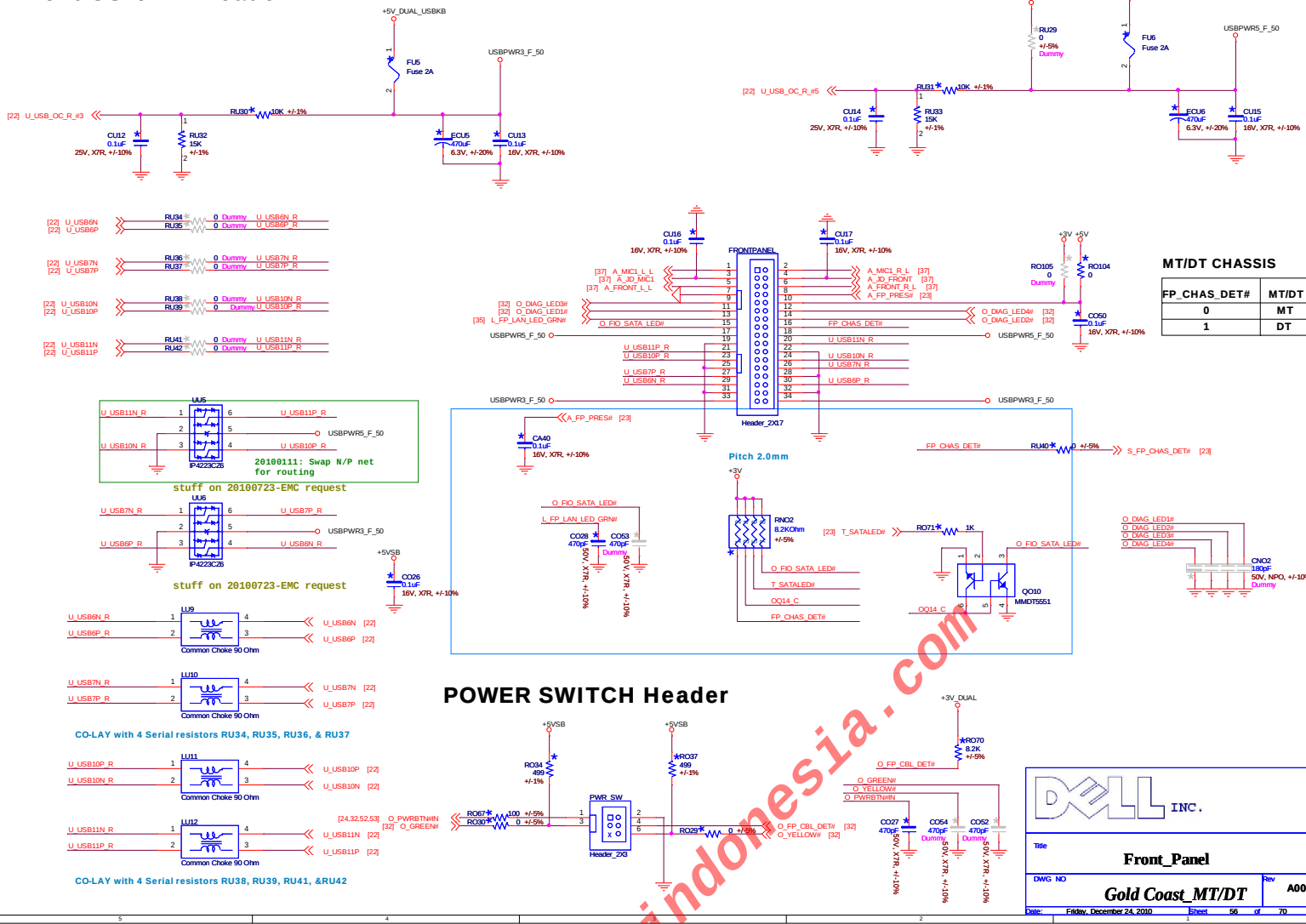
# Front USB/LED Header




# POWER SWITCH Header

## MT/DT CHASSIS

| FP_CHAS_DET# | MT/DT |
|---|---|
| 0 | MT |
| 1 | DT |

DELL INC.

Title: **Front_Panel**

DWG NO: ***Gold Coast_MT/DT***

Rev: A00

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DELL INC.

Title

**TBD**

DWG NO

***Gold Coast_MT/DT***

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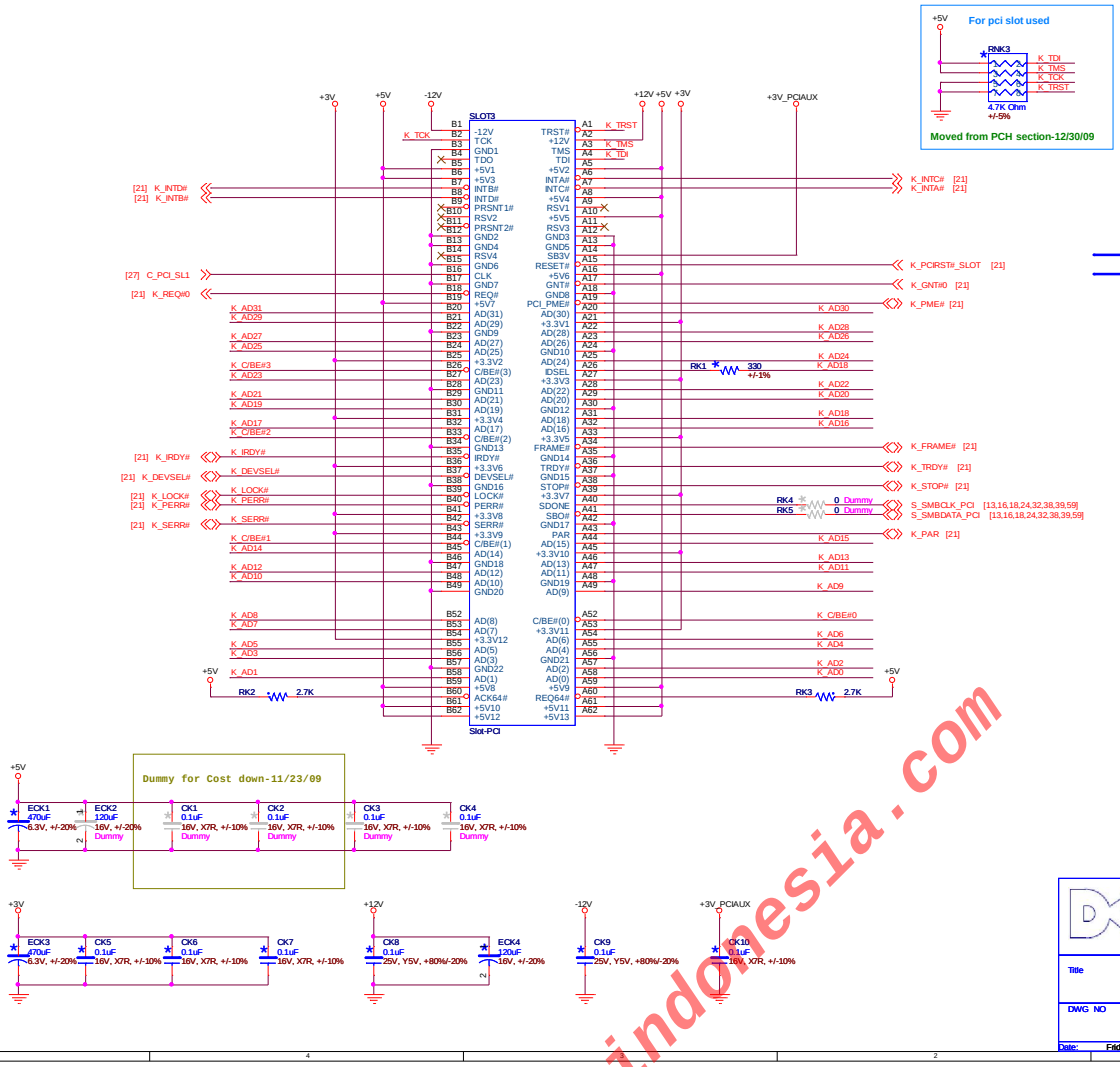
**A00**

Date: Friday, December 24, 2010 Sheet 57 of 70

IRQ: CDAB
IDSEL: AD18
REQ/GNT: 0










DELL INC.

Title: Slot3: PCI

DWG NO: Gold Coast_MT/DT

Rev: A00

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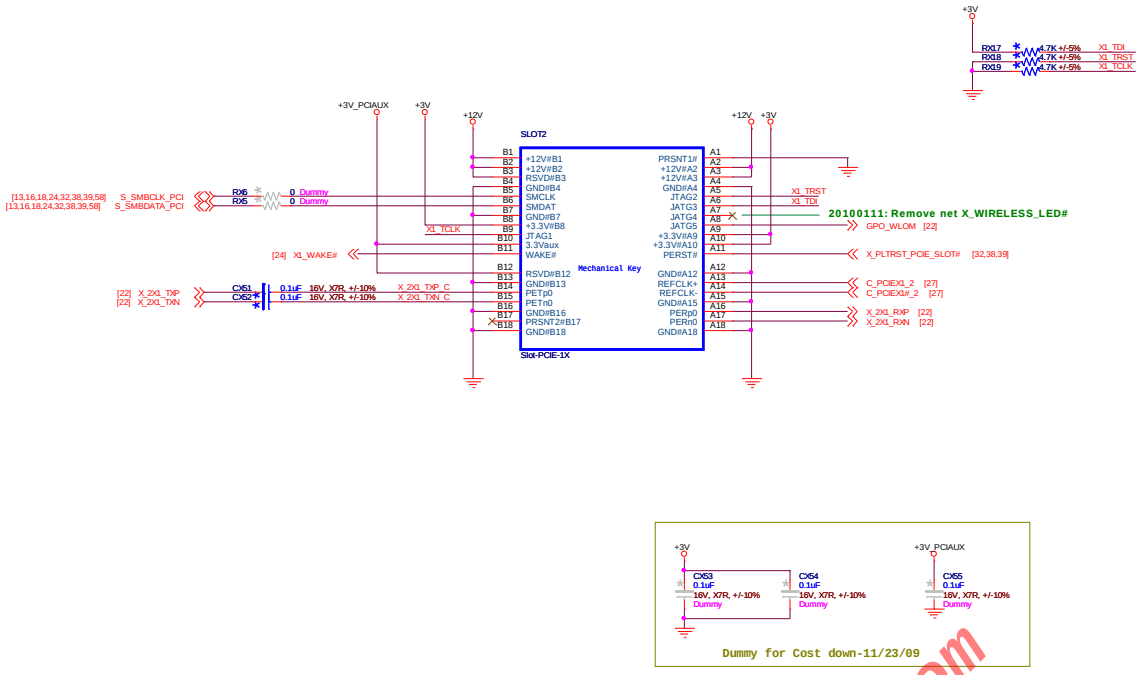







DELL INC.

Title: **Slot2: PCIe 1x**

DWG NO: *Gold Coast_MT/DT*

Rev: A00

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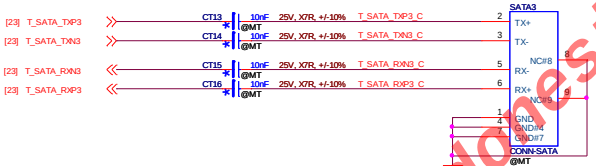
## SATA port 3 only for MT




| | |
|---|---|
| Title | SATA_MT |
| DWG NO | Gold Coast_MT/DT |
| Rev | A00 |
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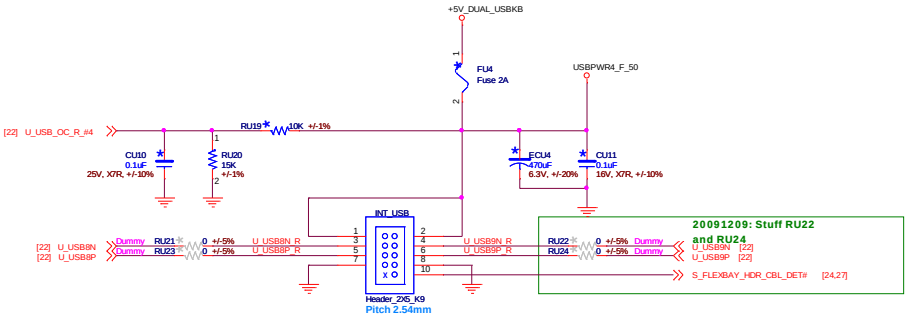
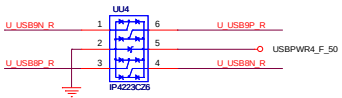
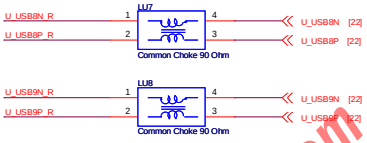
# FLEXBAY




stuff on 20100723-EMC request




CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24



DELL INC.

Title: Flexbay USB

DWG NO: Gold Coast_MT/DT

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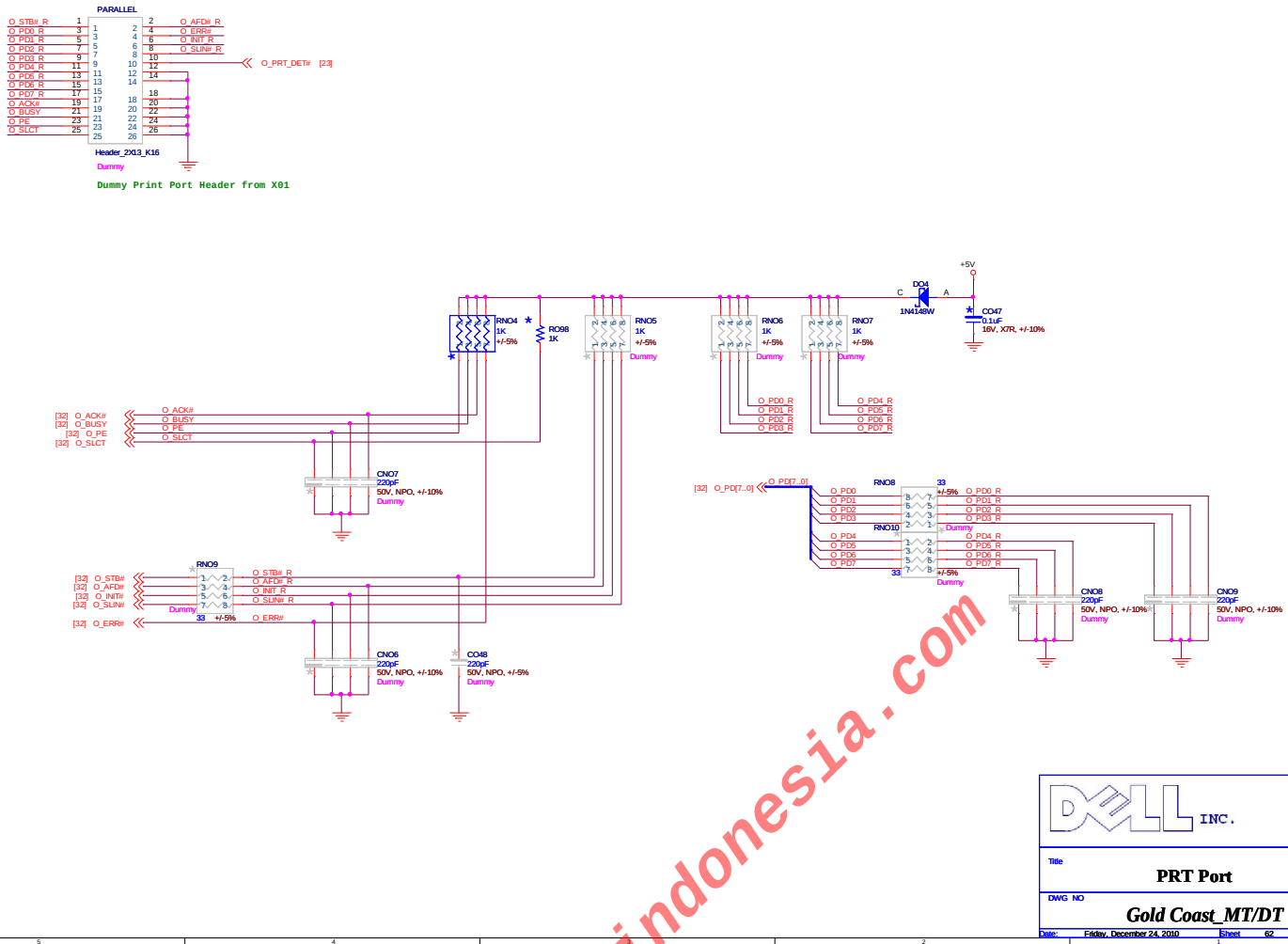
# Print Port






DELL INC.

Title: PRT Port

DWG NO: Gold Coast_MT/DT

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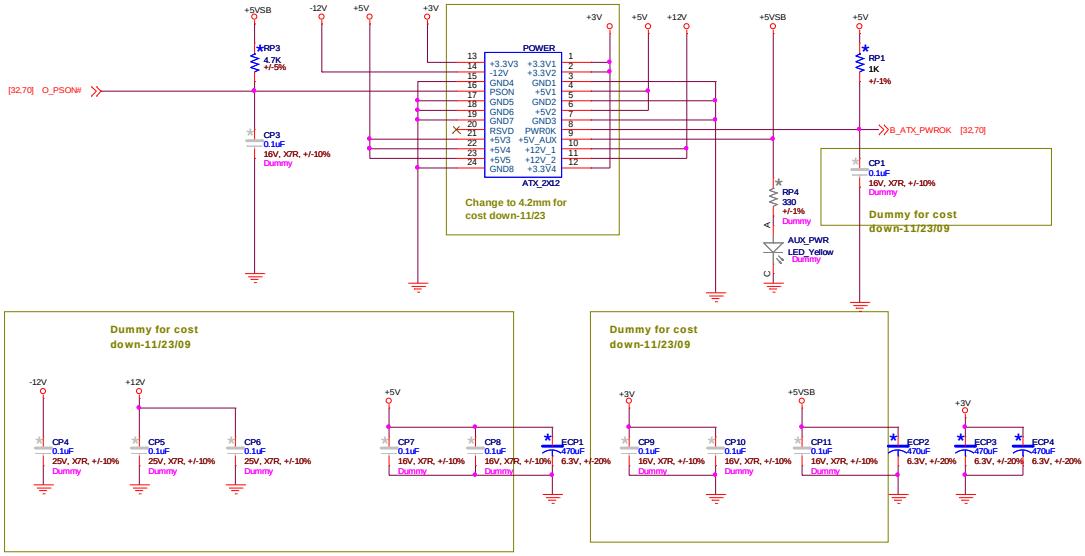
# ATX POWER CONNECTOR









DELL INC.

Title: **Power Conn**

DWG NO: ***Gold Coast_MT/DT***

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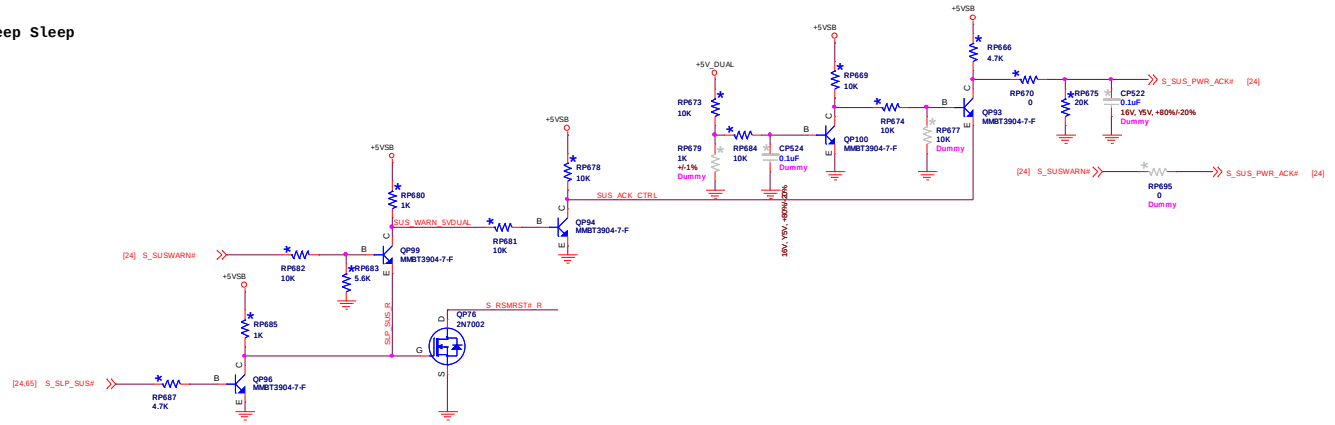
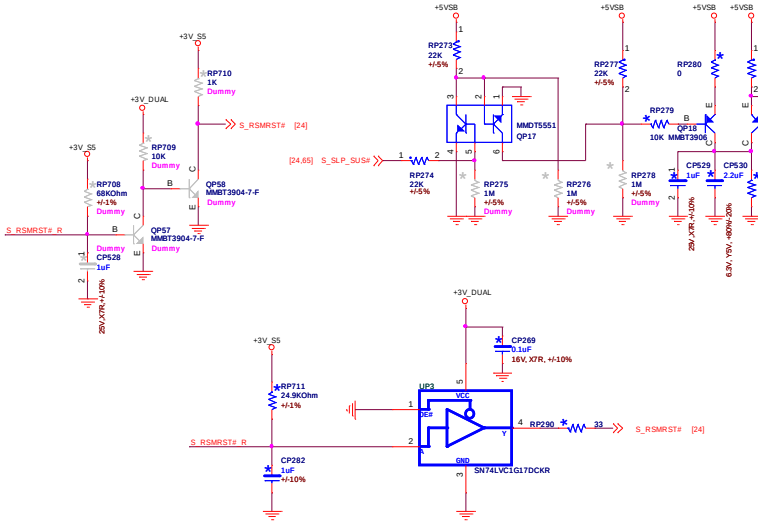
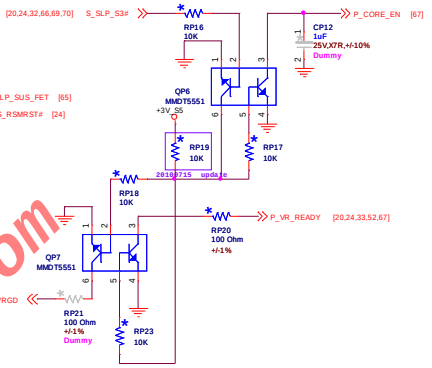
## For Deep Sleep




## RESUME RESET Logic




## VR_READY DEFENSIVE




| | |
|---|---|
| Title | Power Sequence |
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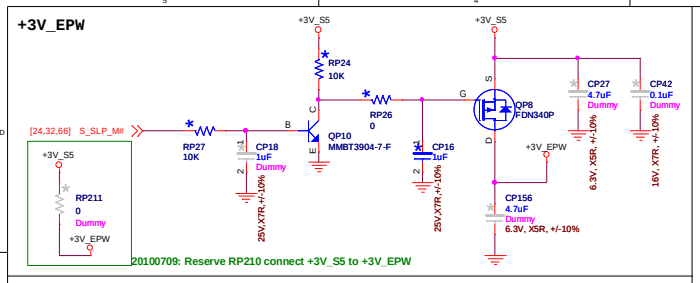


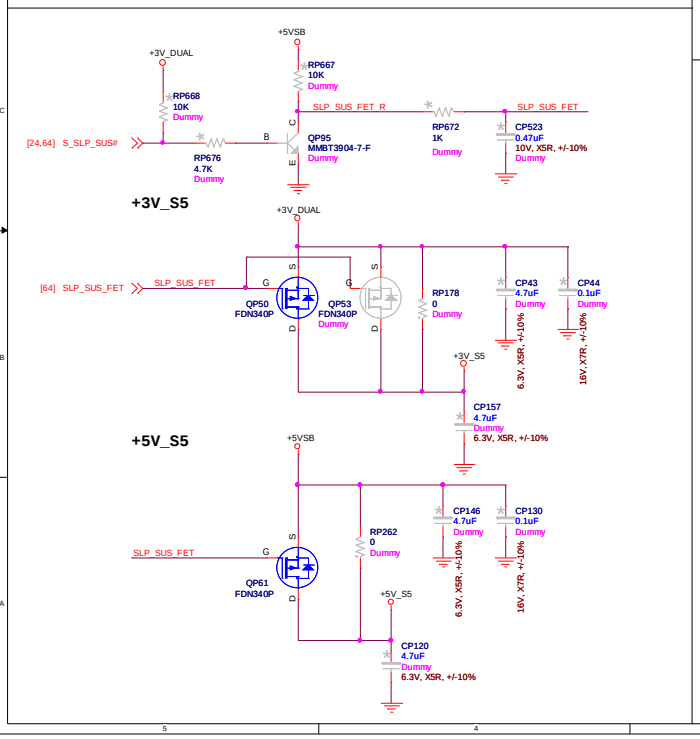


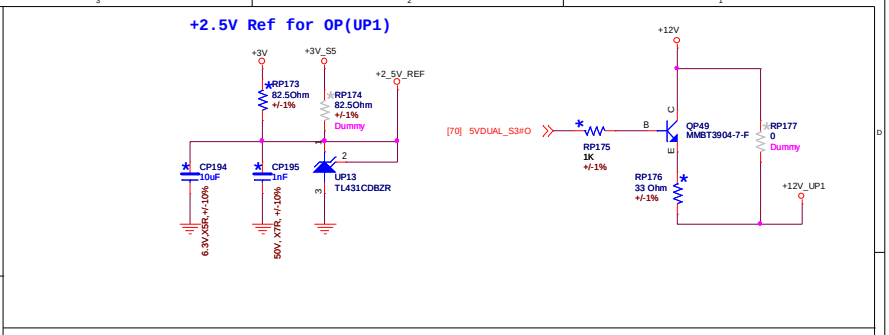


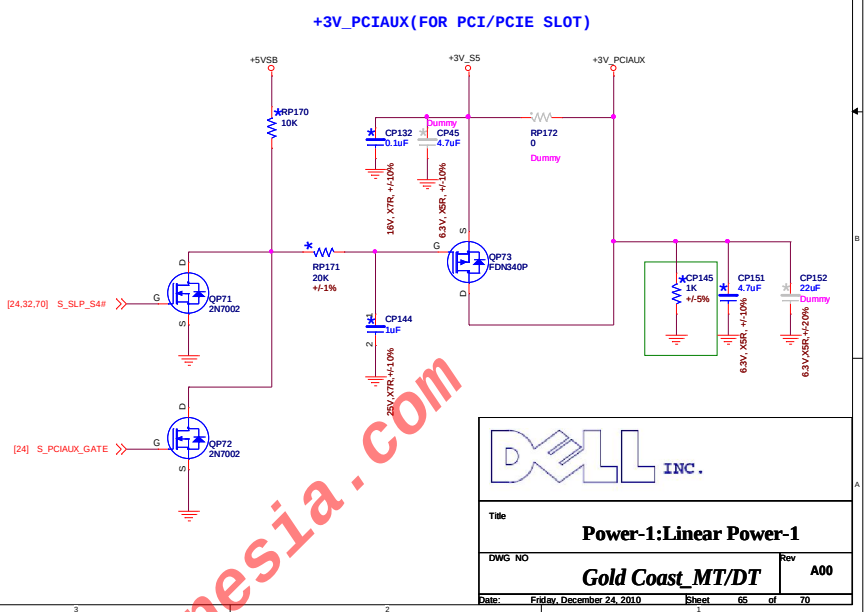


DELL INC.

Title: Power-1:Linear Power-1

DWG NO: Gold Coast_MT/DT

Rev: A00

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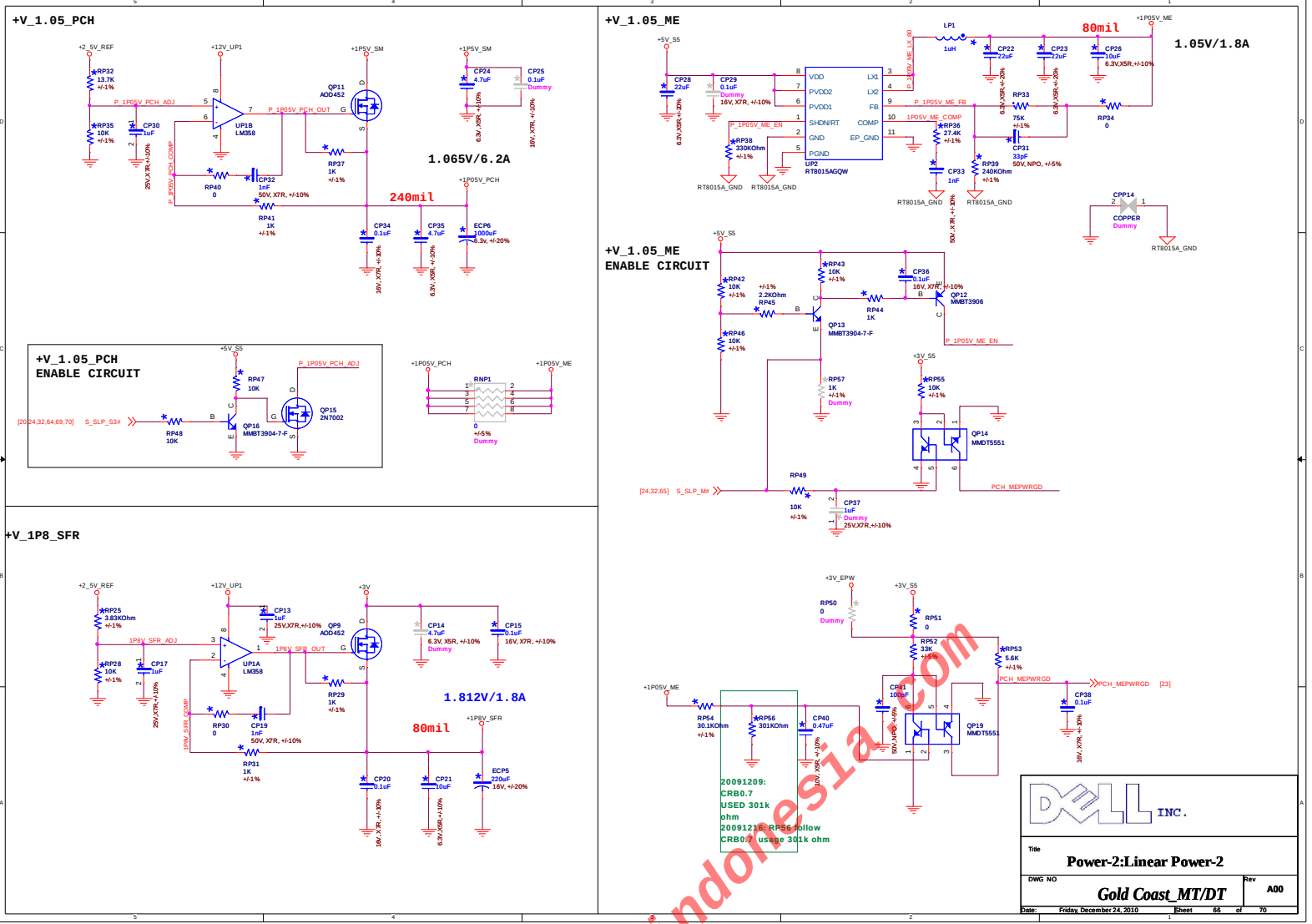

# Sugar Bay VR12 POWER - 4+1 PHASE

## VCC_CORE

## VCC_AXG

| PWM ADDRESS | | |
|---|---|---|
| RESISTOR VALUE | SVID ADDRESS FOR VCORE RAIL | SVID ADDRESS FOR V_GT RAIL |
| 10K | 0000 | 0001 |
| 25K | 0010 | 0011 |
| 45K | 0100 | 0101 |
| 70K | 0110 | 0111 |
| 95K | 1000 | 1001 |
| 125K | 1010 | 1011 |
| 165K | 1100 | 1101 |

| BOOT VOLTAGE | |
|---|---|
| RESISTOR VALUE | BOOT VOLTAGE |
| 10K | 0V |
| 25K | 0.85V |
| 45K | 0.9V |
| 70K | 0.95V |
| 95K | 1V |
| 125K | 1.1V |
| 165K | 1.5V |

3PHASE OPTION

VCORE VBOOT SET AT 0V

V_GT IMAX SET AT 35A

PWM ADDRESS

VCORE IMAX SET AT 120A

7X7 SINGLE ROW QFN

VCORE PORTION

V_GT PORTION

OPTION: DISALBE V_GT

PUT COLSE TO V_GT HOT SPOT

Work F= 300Khz

BOTTOM PAD CONNECT TO GND Through 4 VIAs

PUT COLSE TO VCORE HOT SPOT

Set 110deg OTP

Green mark is update from 20100720

Green mark is update from 20100726

Green mark is update from 20100830

Green mark is update from 20101012

DELL INC.

Title: Power-3: Vcore PWM

DWG NO: Gold Coast_MT/DT

Rev: A00

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